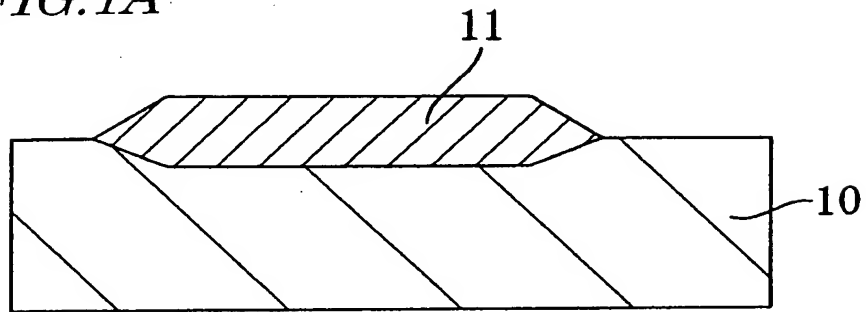
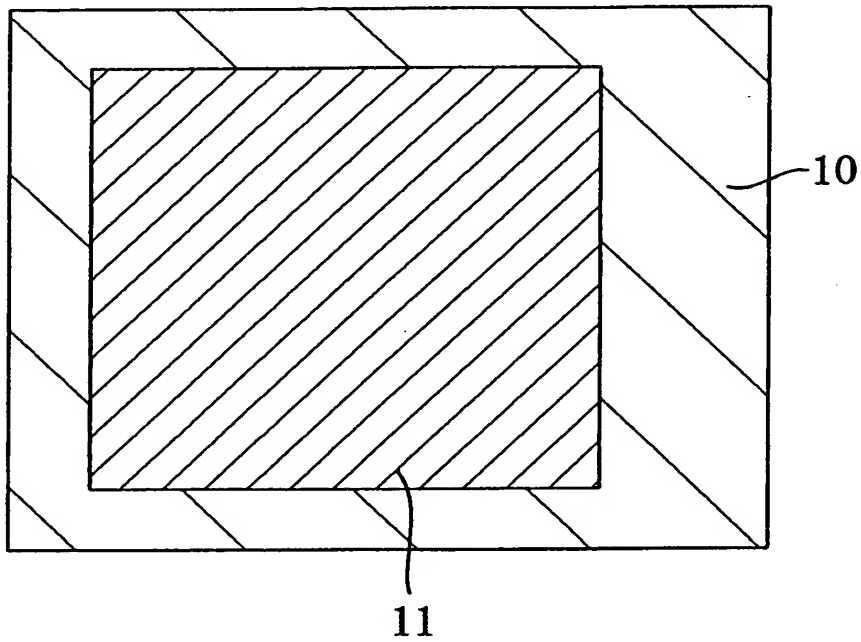


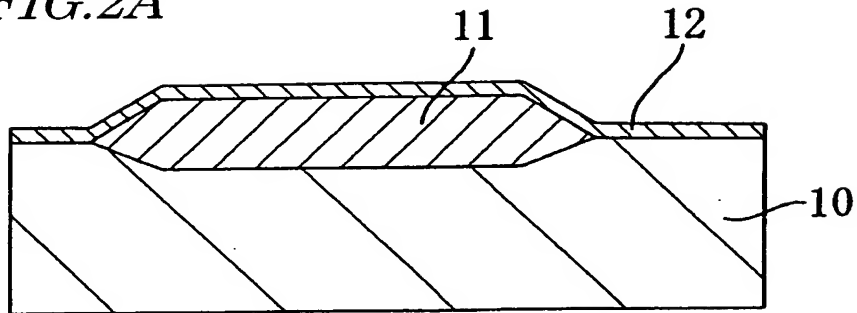
*FIG. 1A*



*FIG. 1B*



*FIG. 2A*



*FIG. 2B*

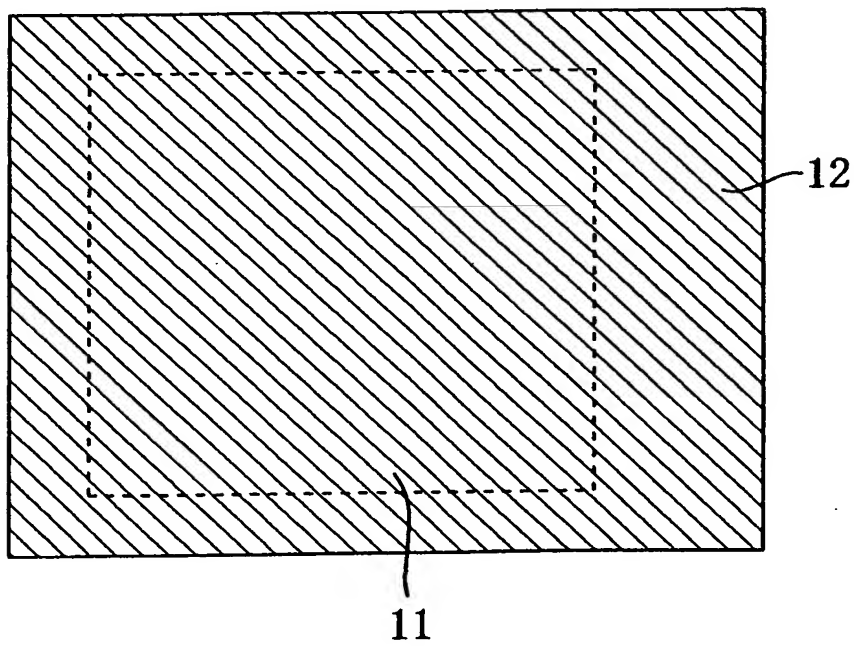


FIG. 3A

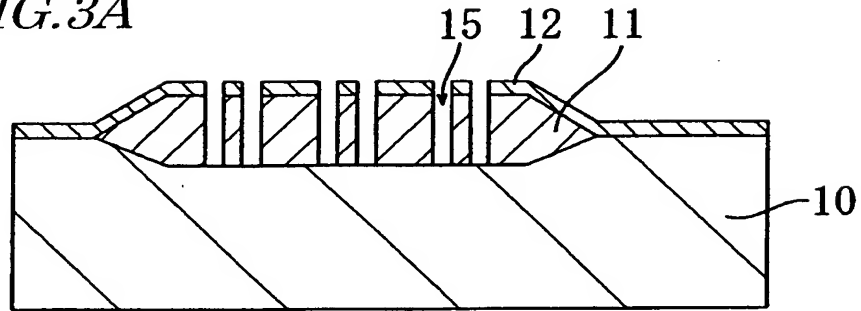


FIG. 3B

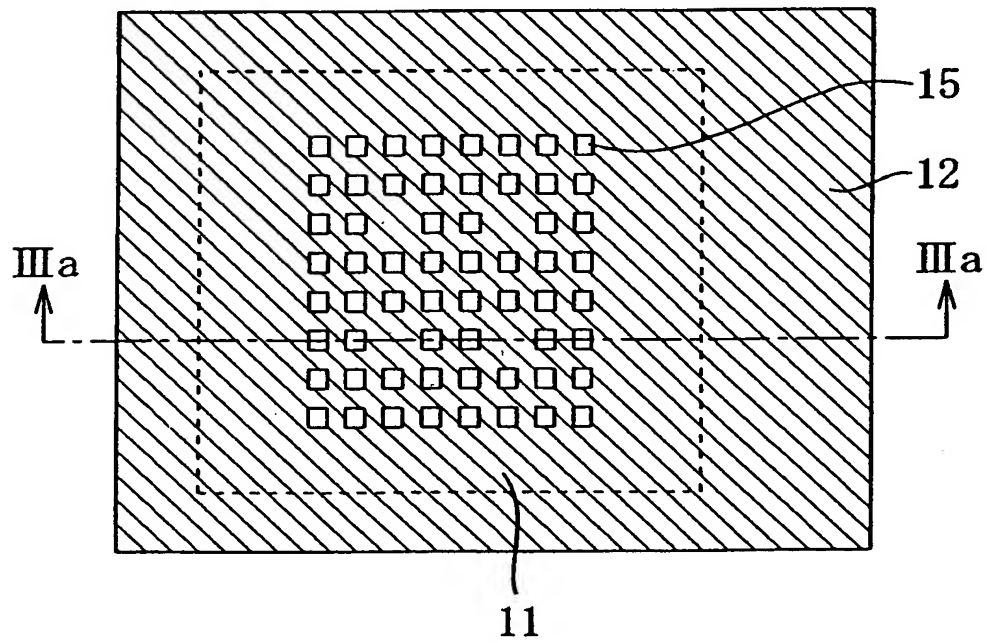


FIG.4A

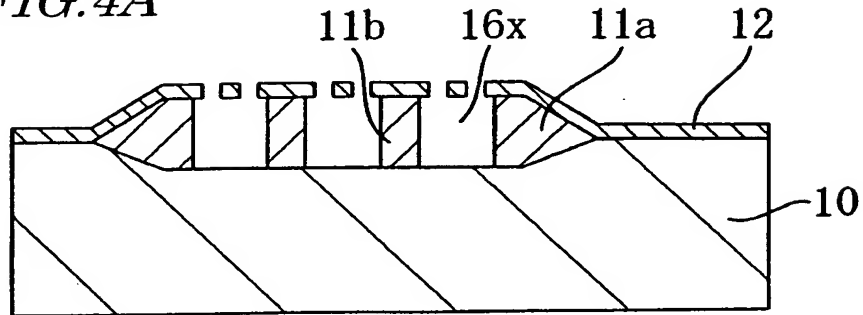


FIG.4B

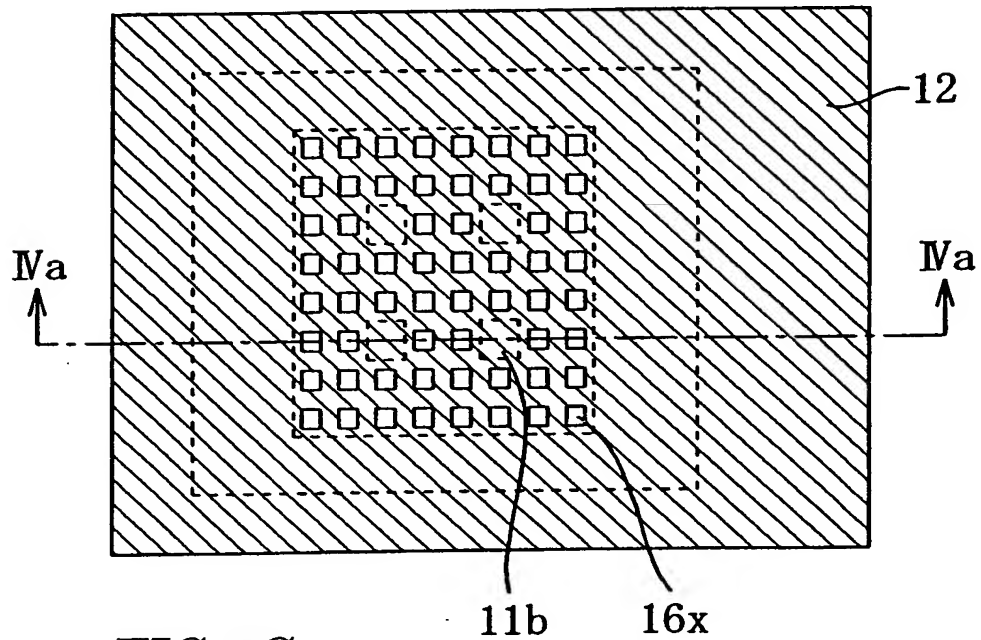
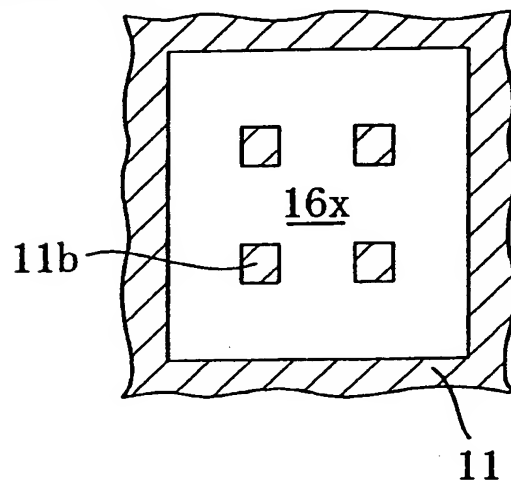
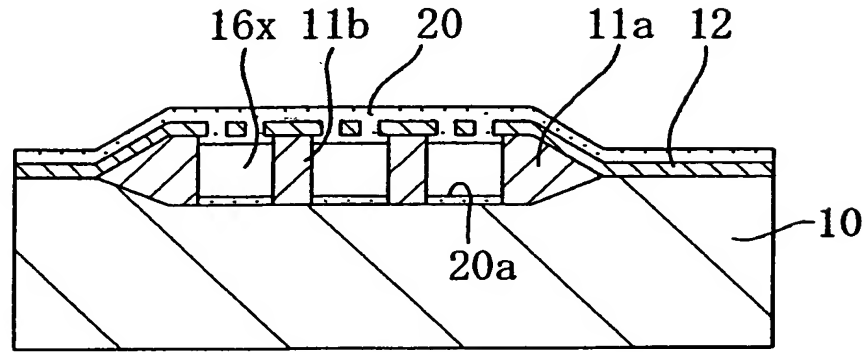


FIG.4C



*FIG. 5A*



*FIG. 5B*

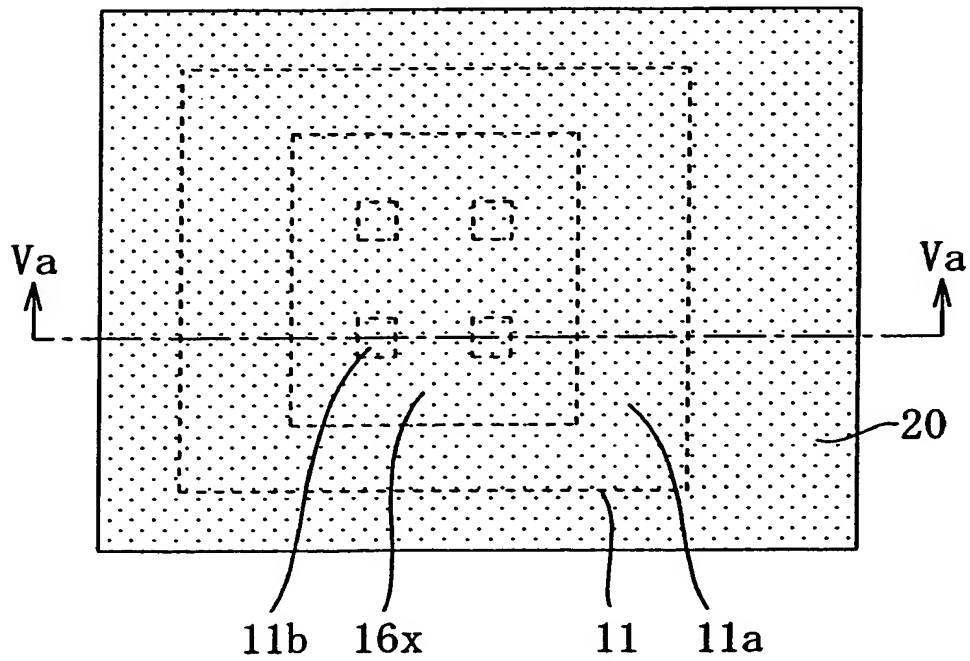


FIG. 6A

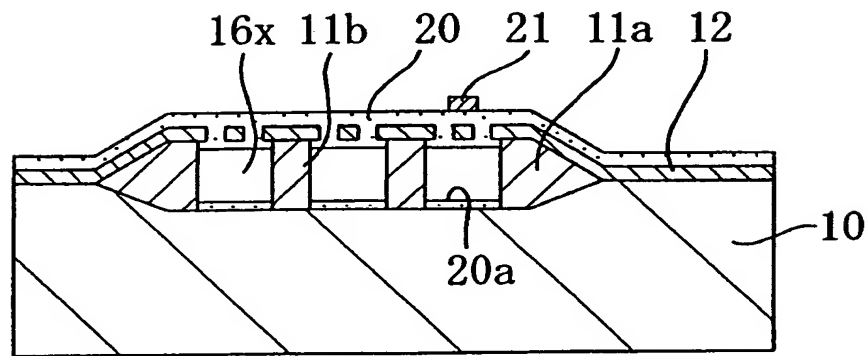
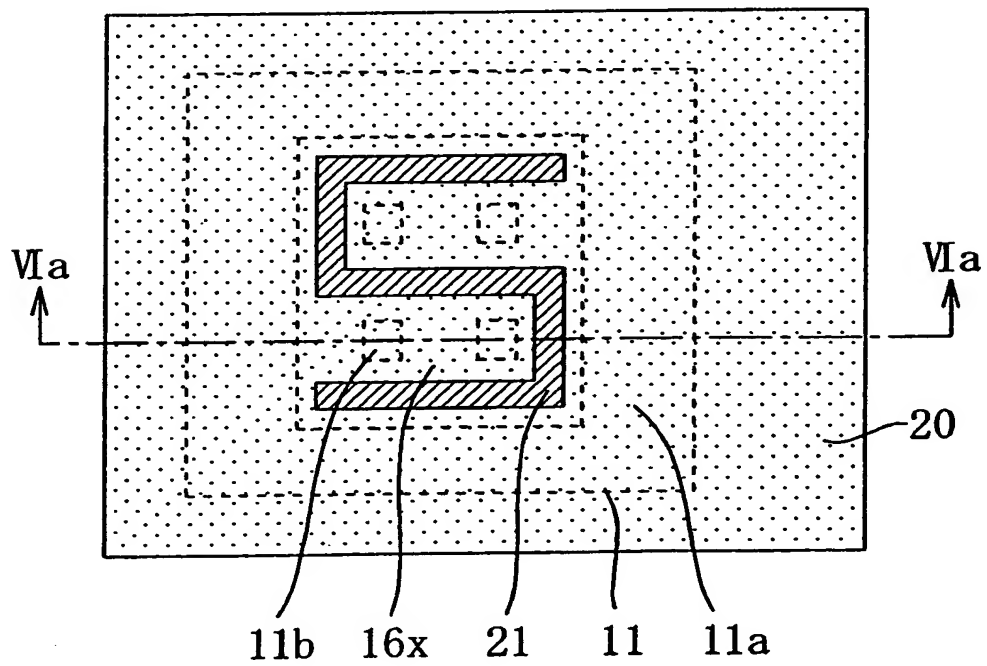
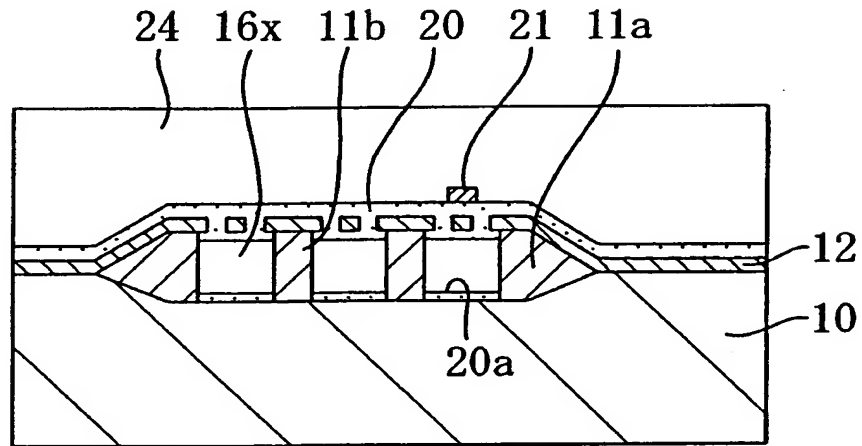


FIG. 6B



*FIG. 7A*



*FIG. 7B*

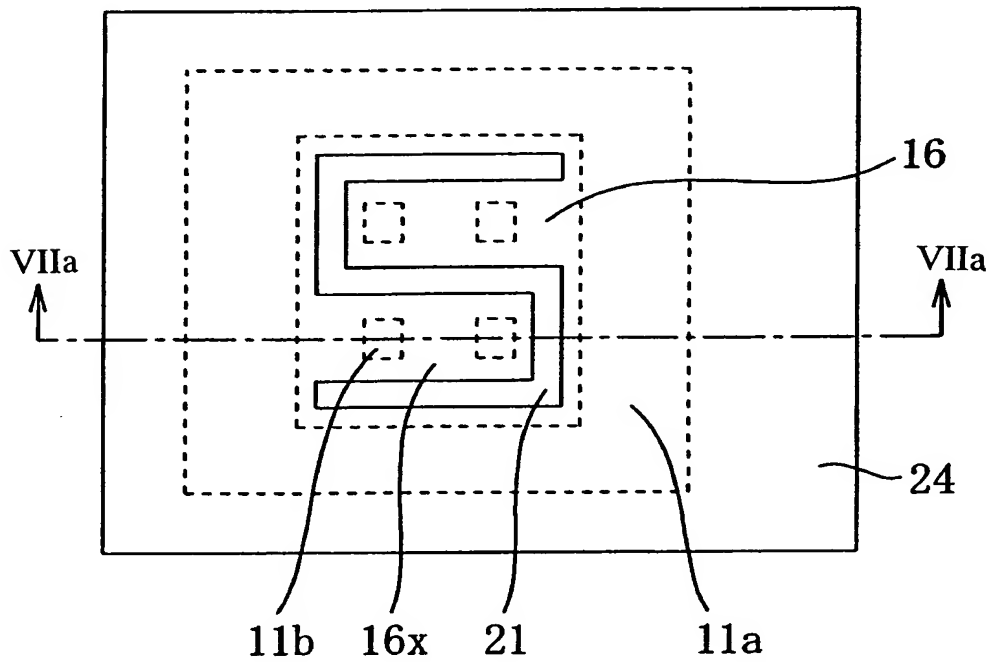
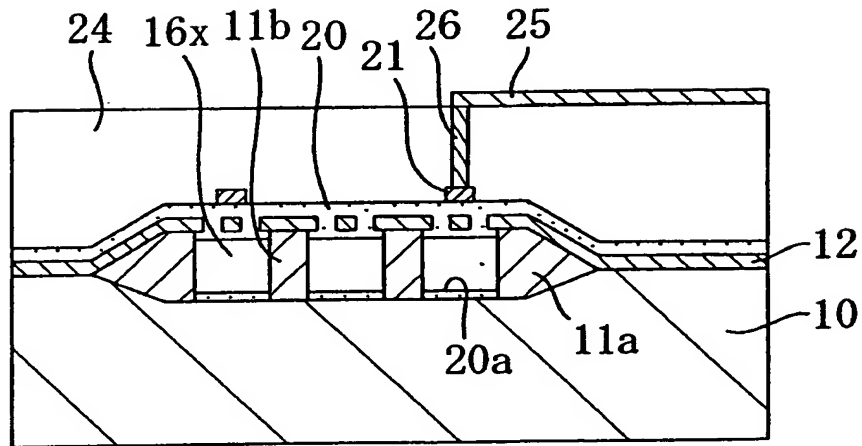


FIG. 8A



*FIG. 8B*

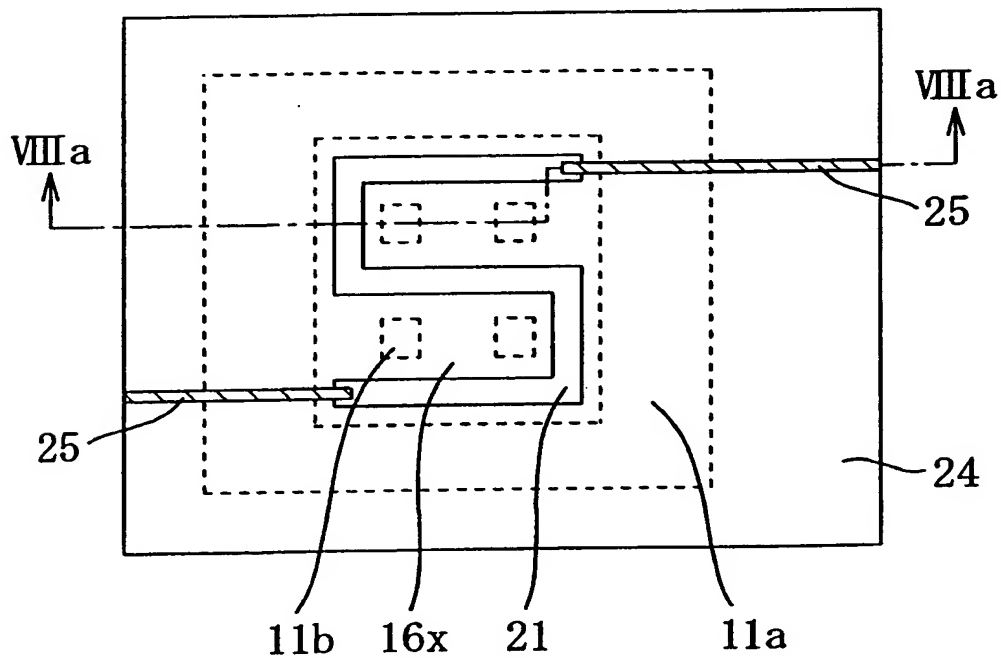




FIG. 9A

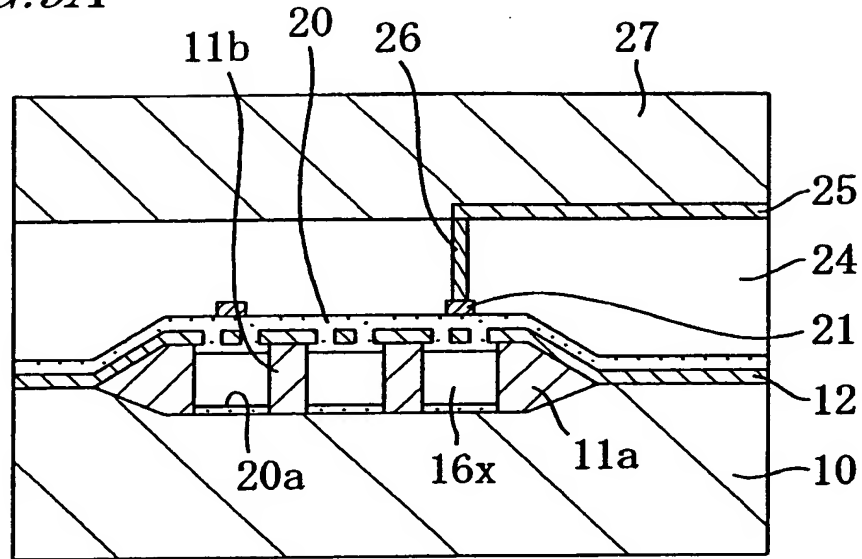
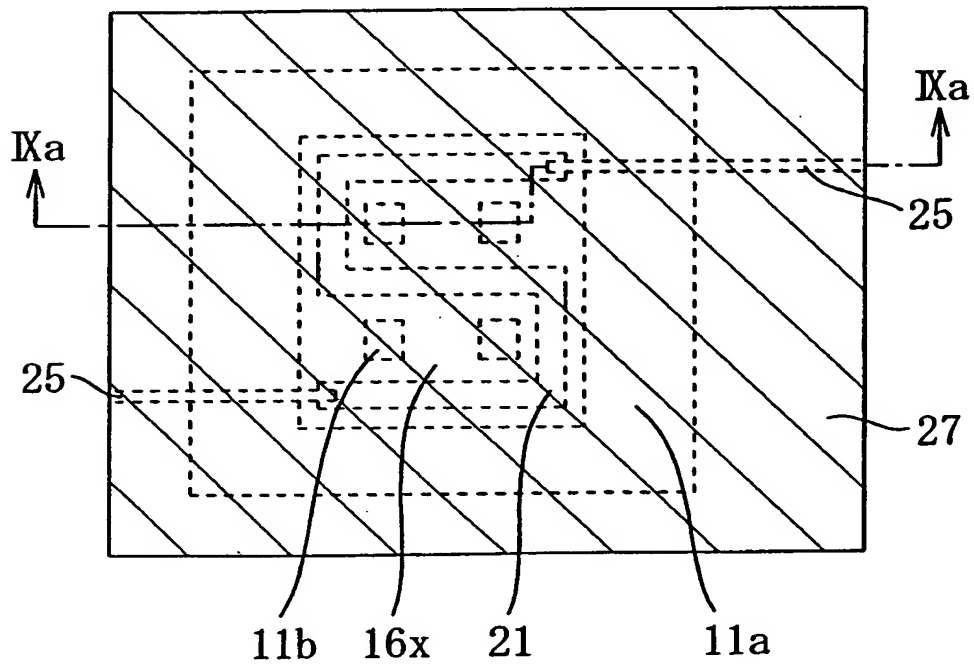
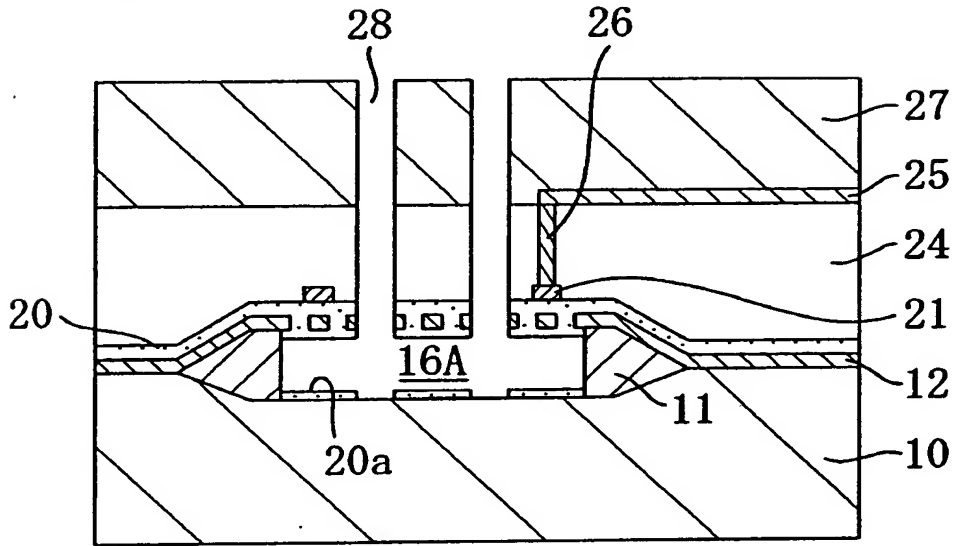


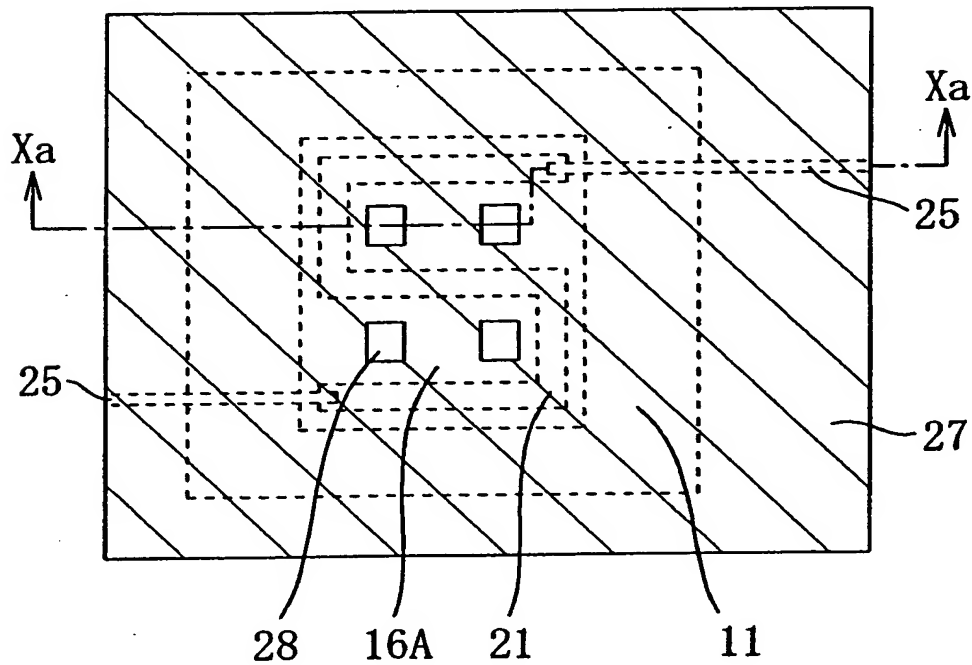
FIG. 9B



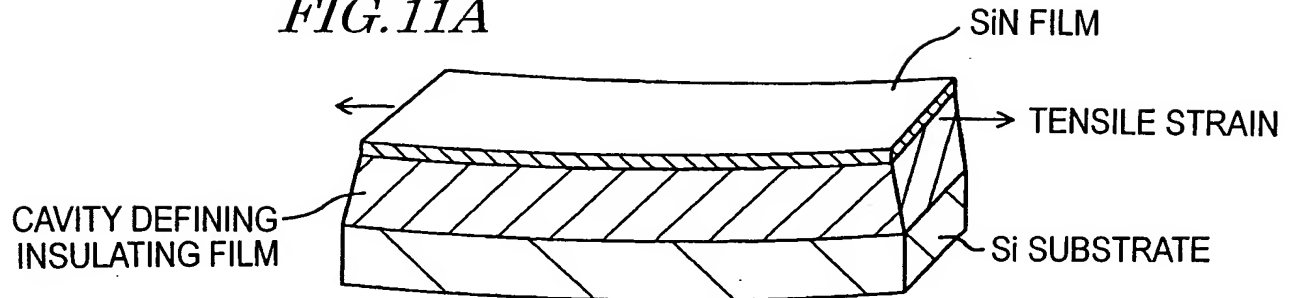
*FIG. 10A*



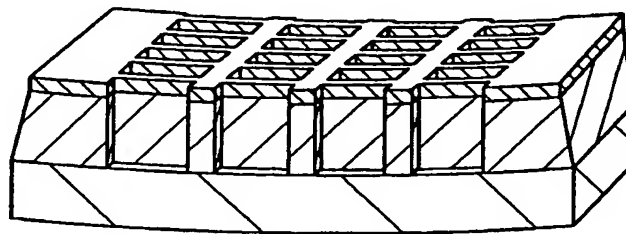
*FIG. 10B*



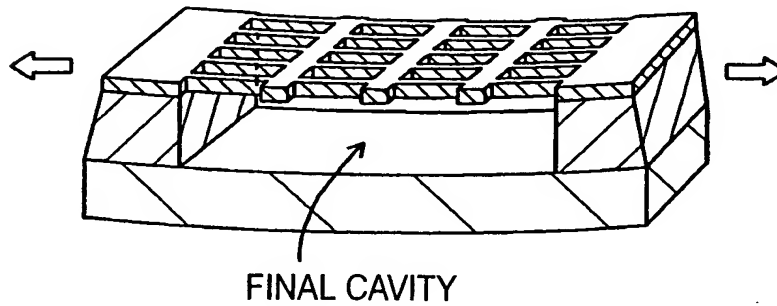
*FIG. 11A*



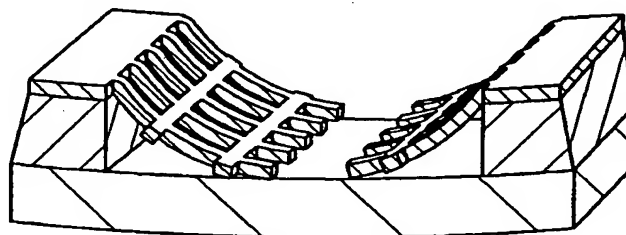
*FIG. 11B*



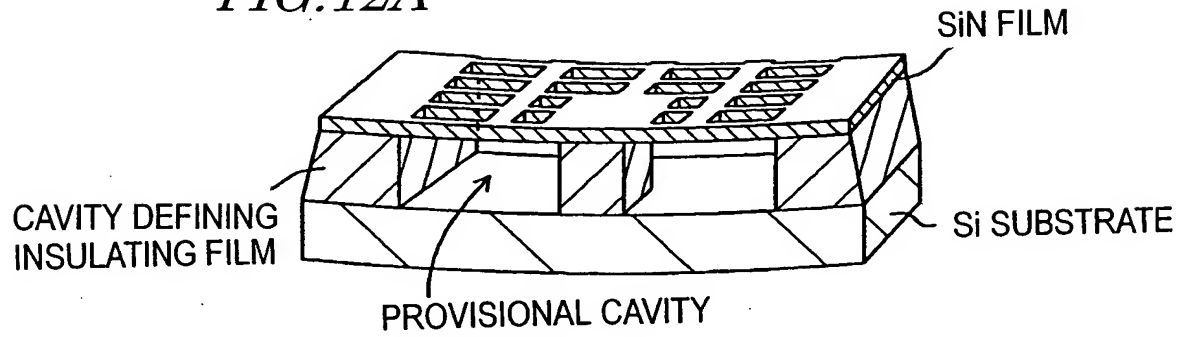
*FIG. 11C*



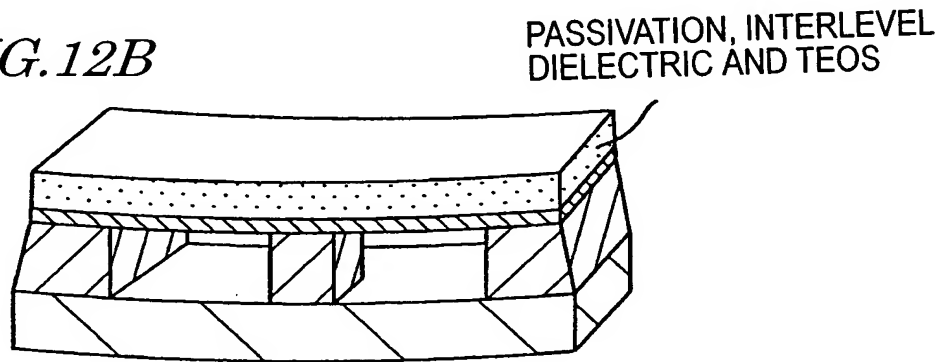
*FIG. 11D*



*FIG. 12A*



*FIG. 12B*



*FIG. 12C*

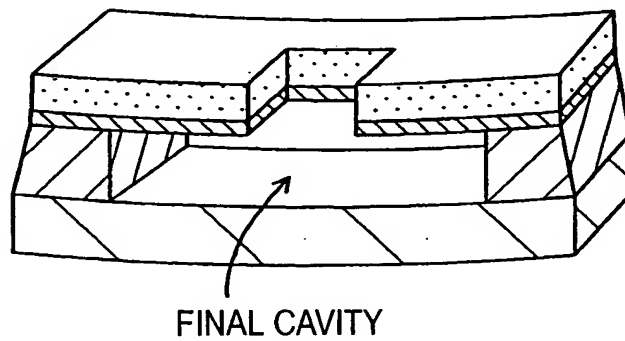


FIG.13A

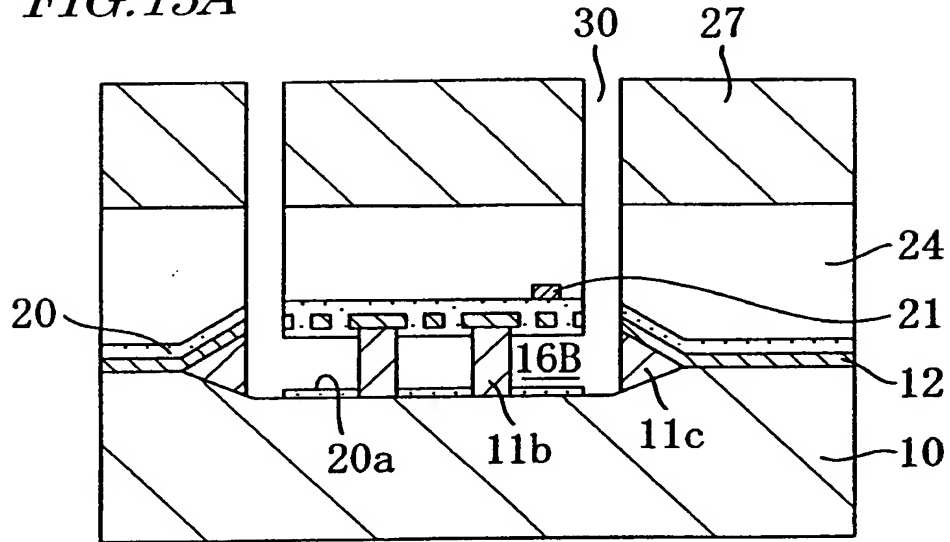
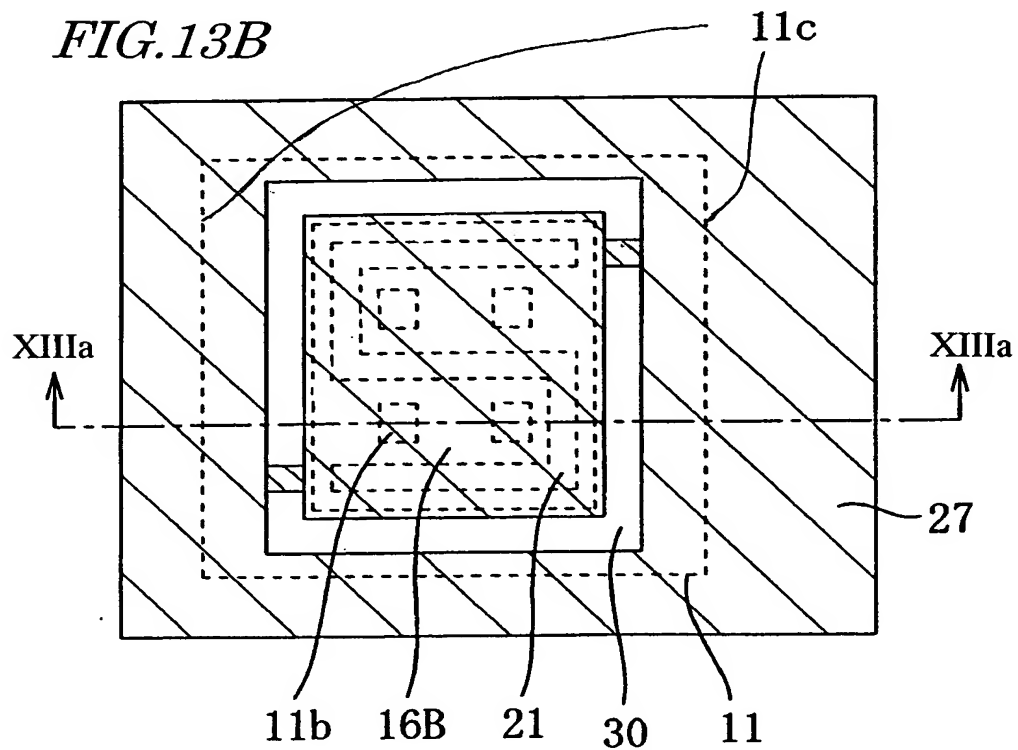
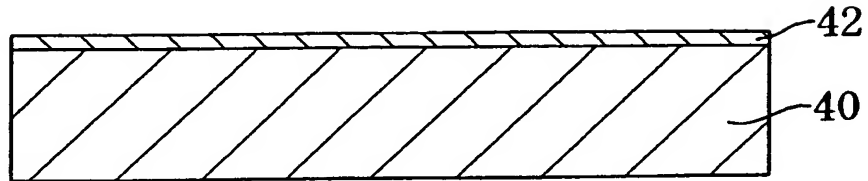


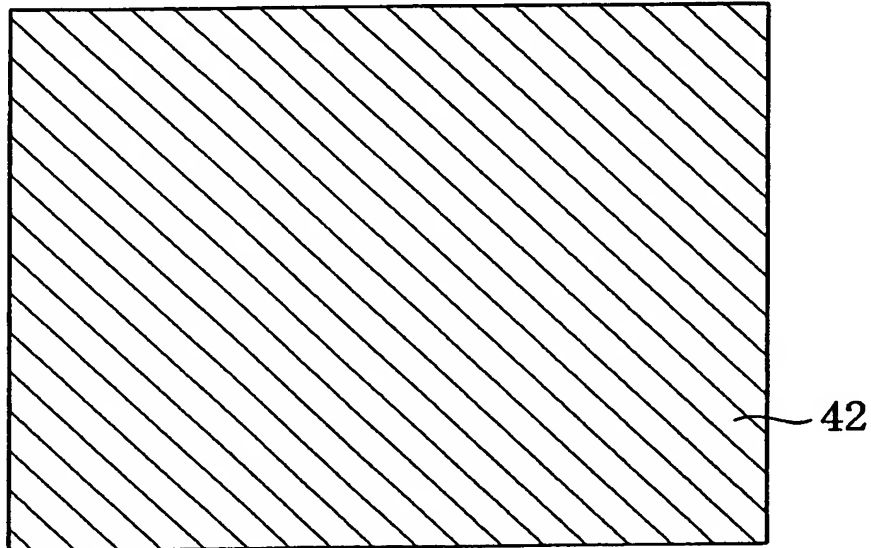
FIG.13B



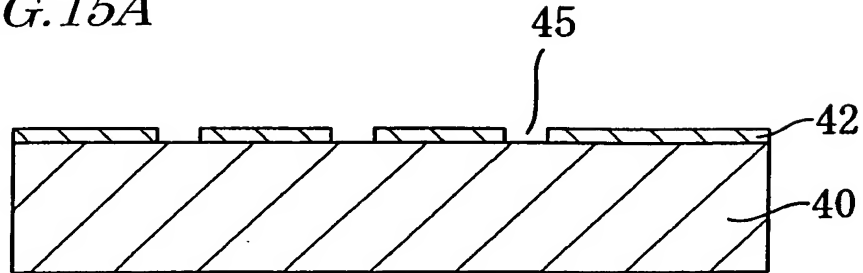
*FIG. 14A*



*FIG. 14B*



*FIG. 15A*



*FIG. 15B*

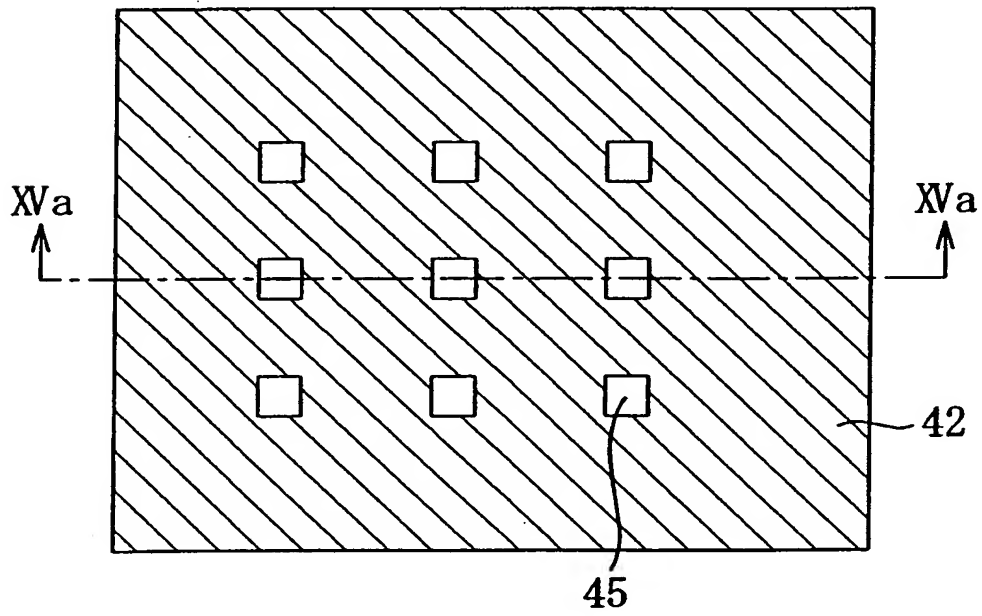


FIG. 16A

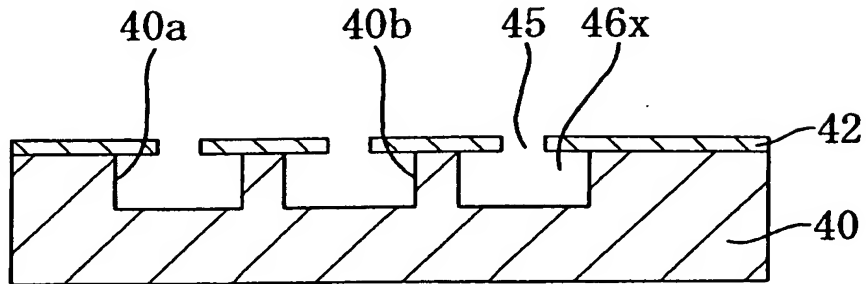


FIG. 16B

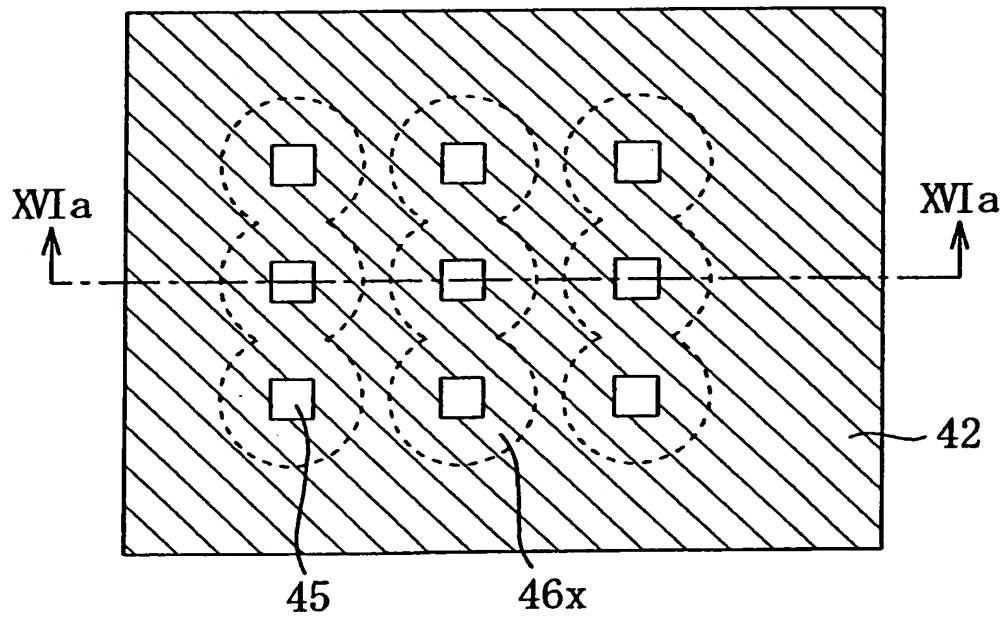




FIG.17A

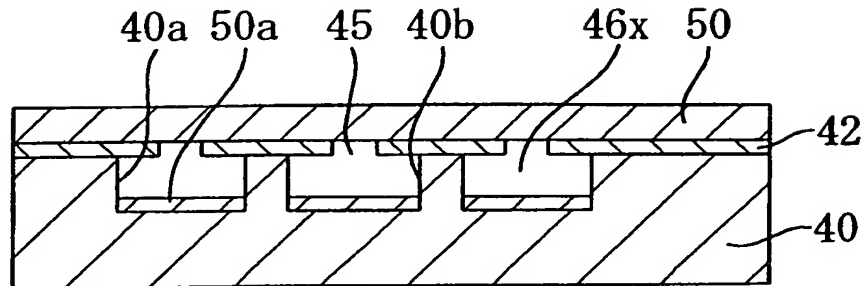


FIG.17B

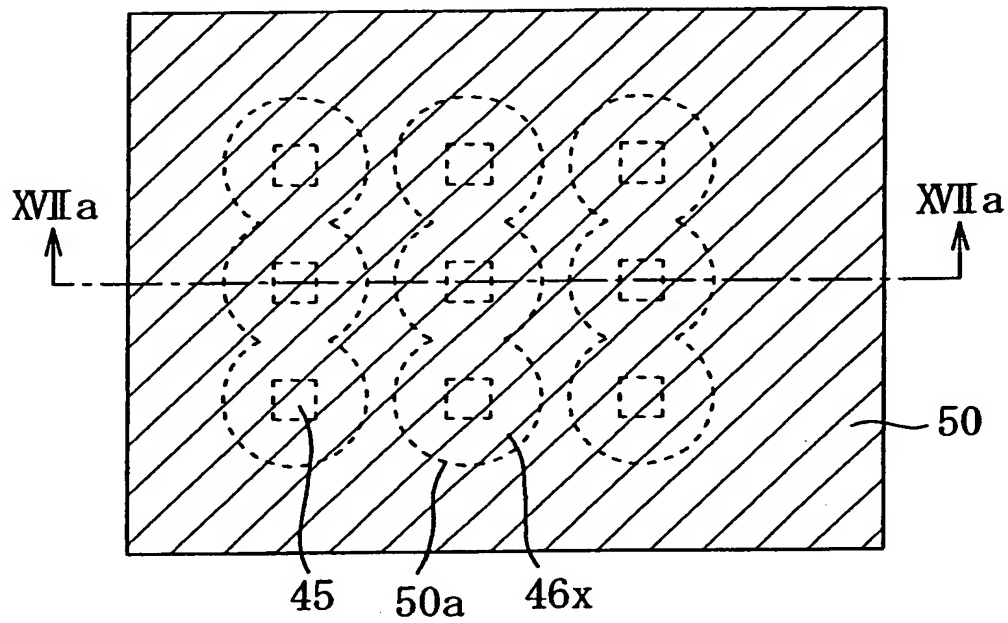


FIG.18A

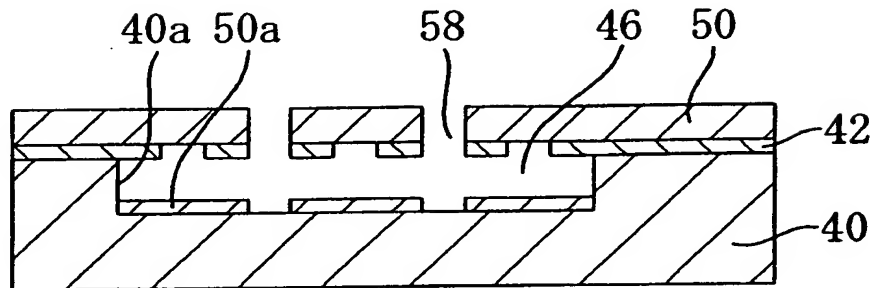


FIG.18B

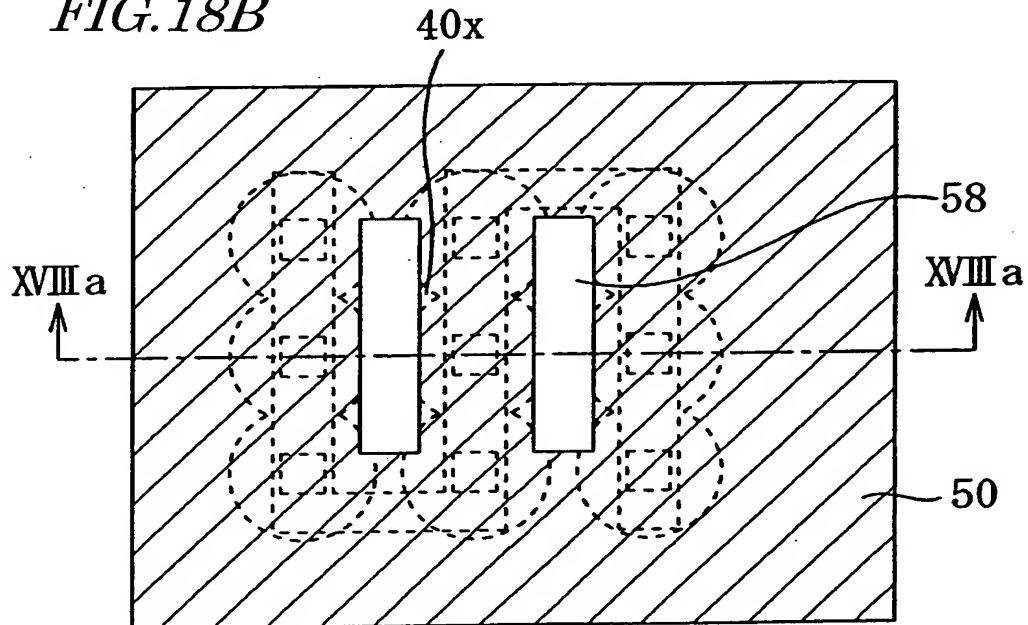




FIG.20A

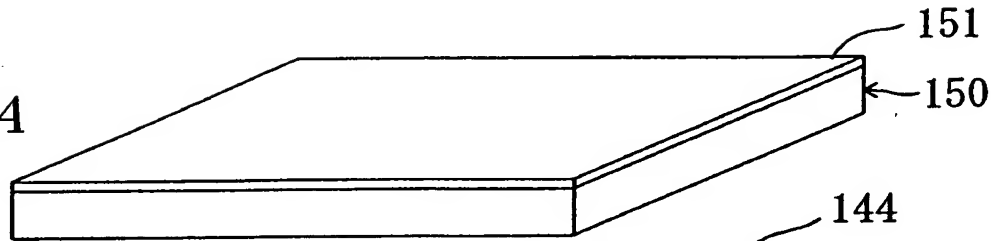


FIG.20B

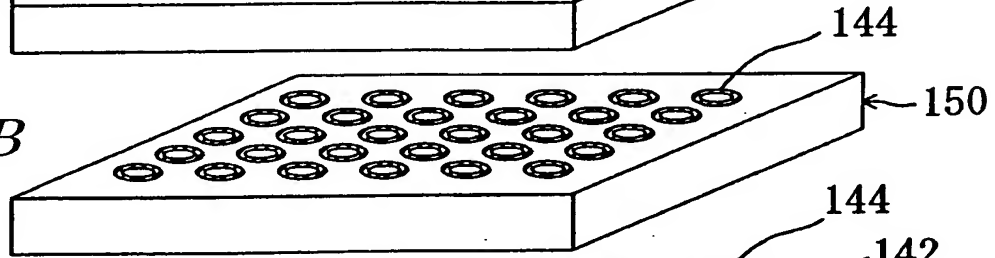


FIG.20C

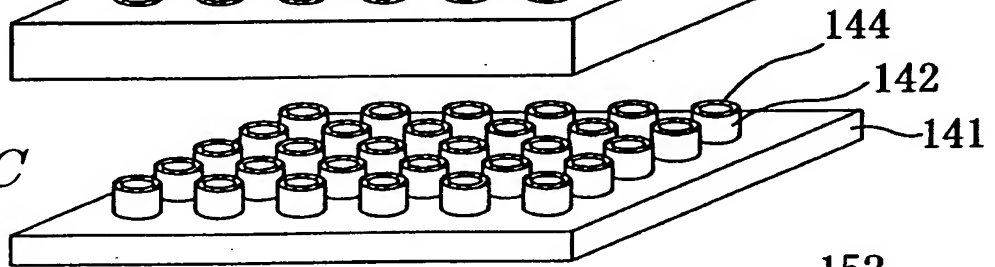


FIG.20D

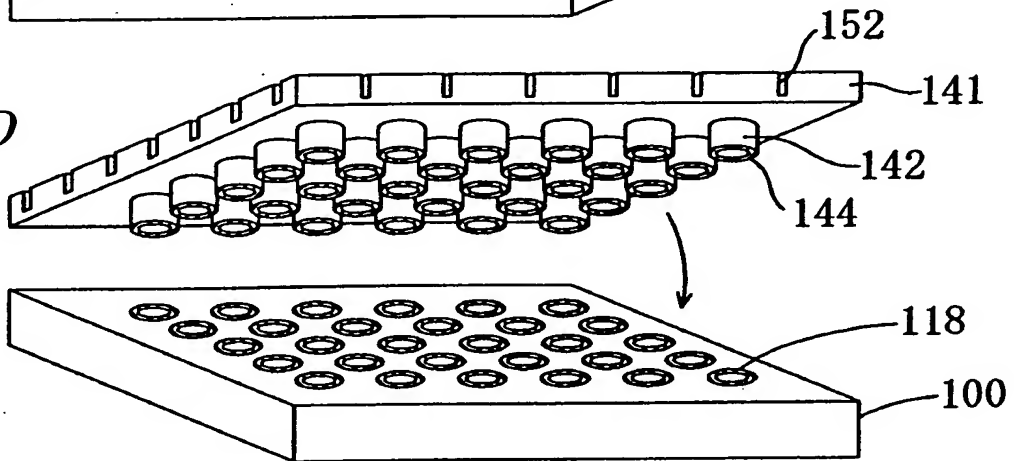


FIG.20E

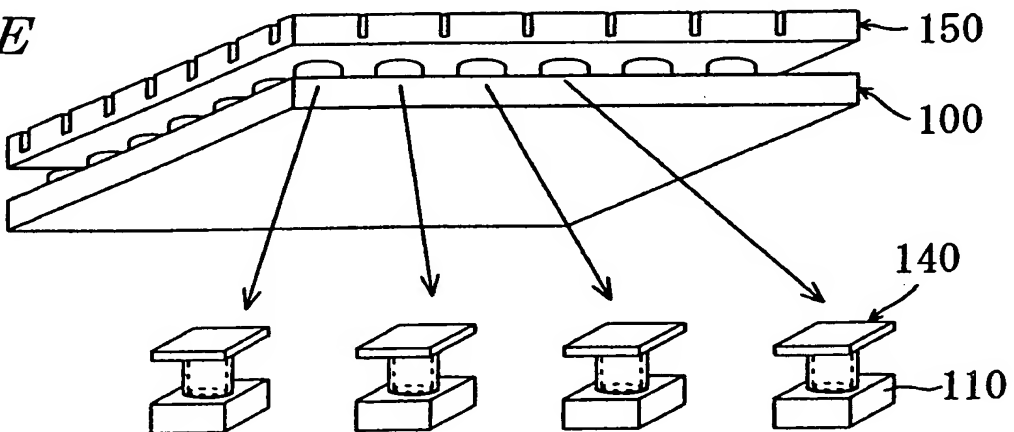
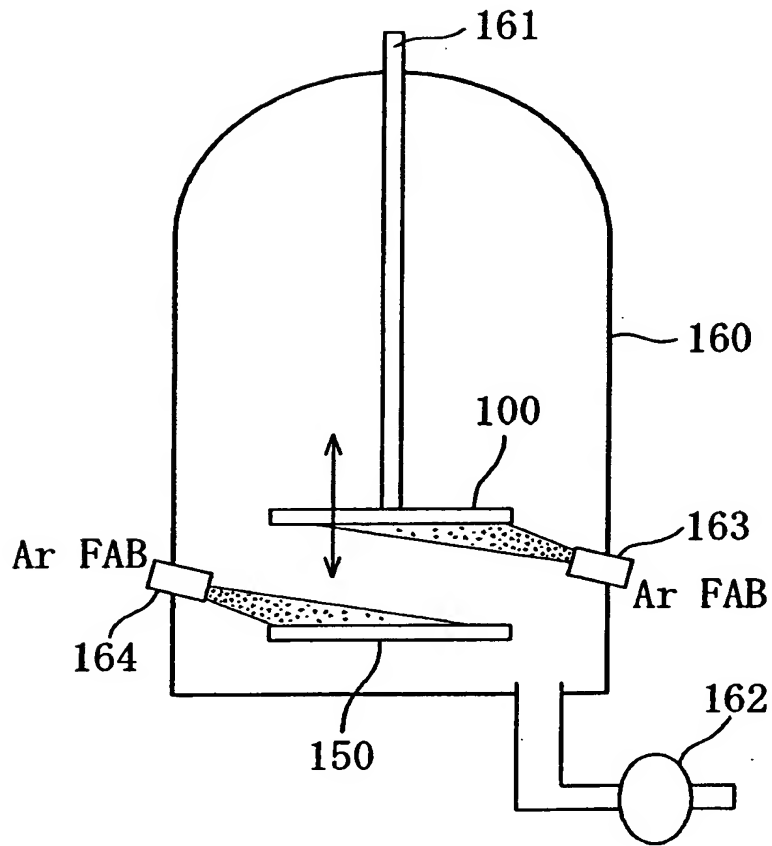
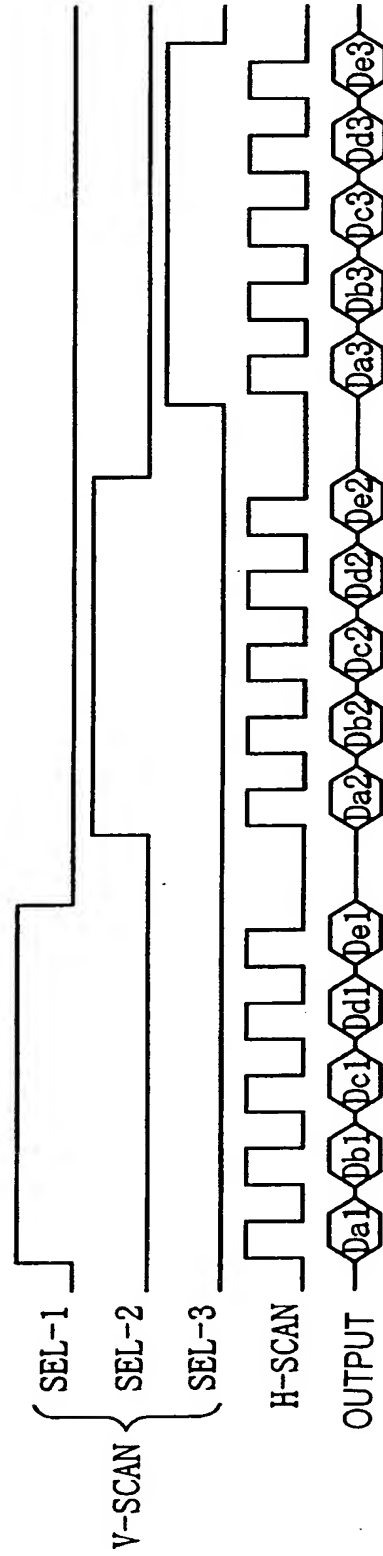


FIG. 21

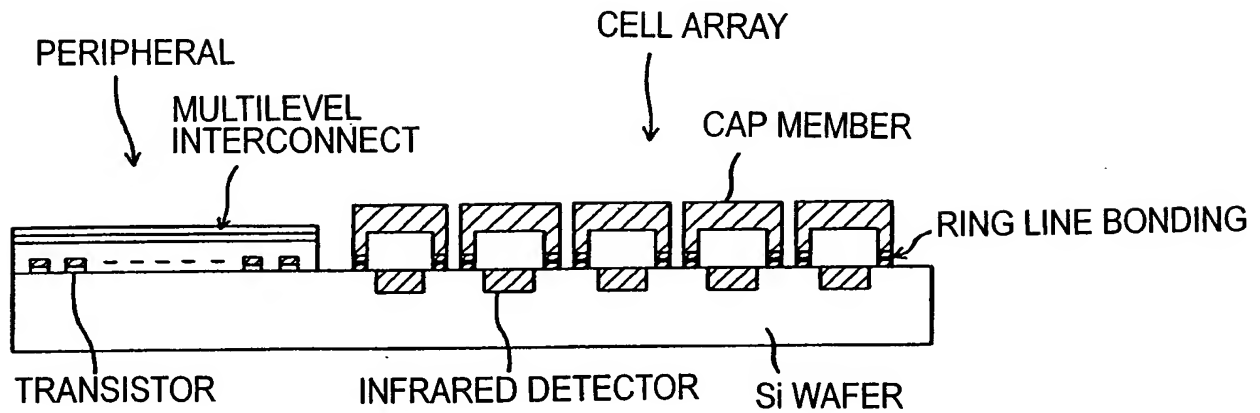


[illegible]

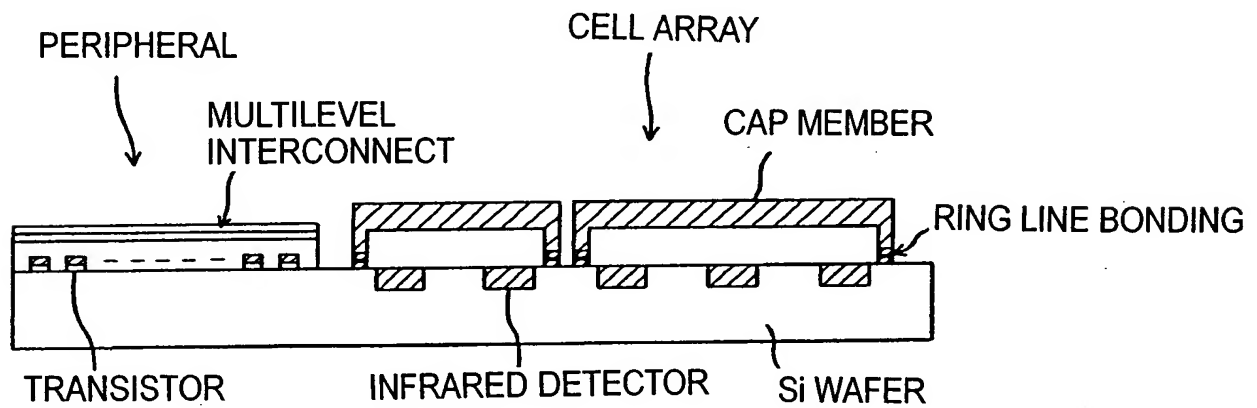
FIG.23



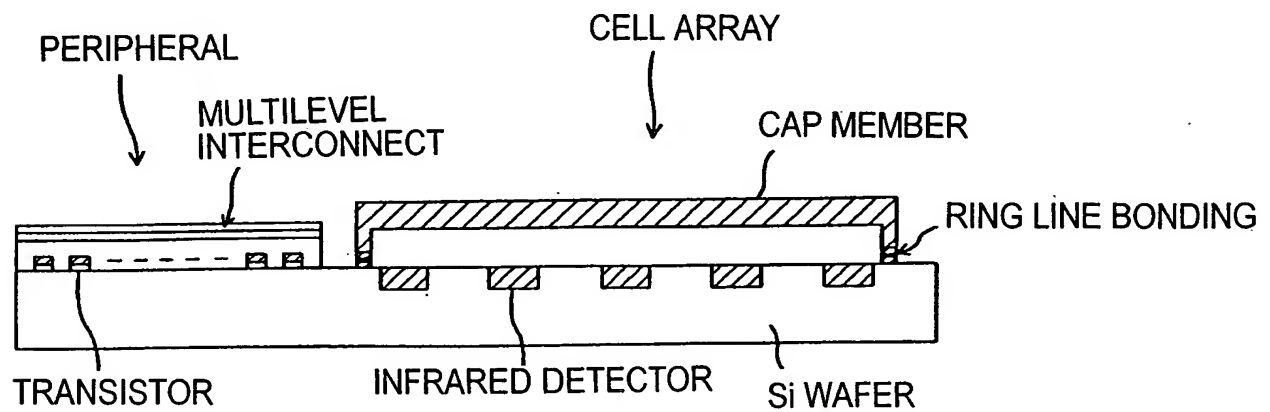
**FIG.24**



**FIG.25**



**FIG.26**





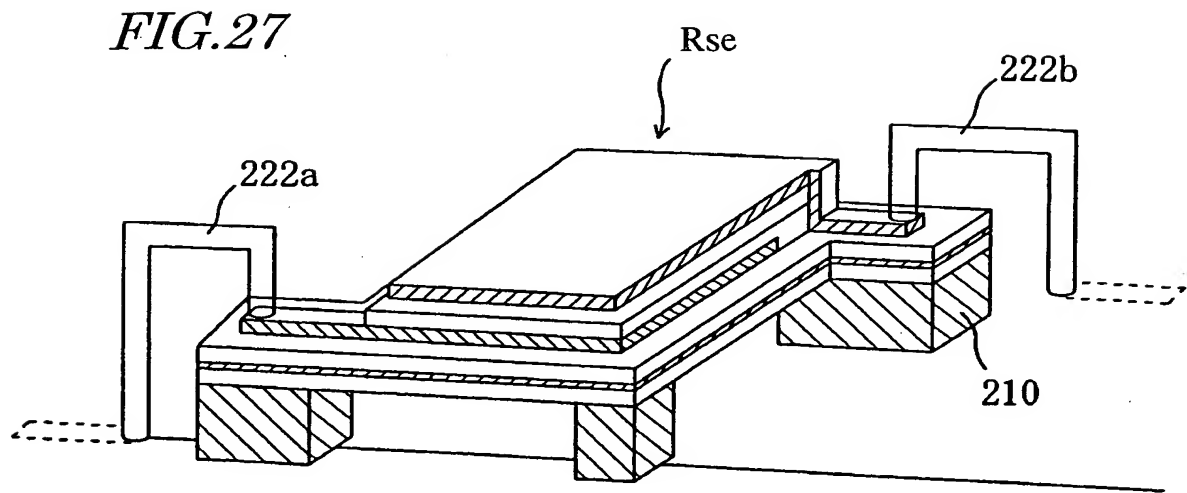
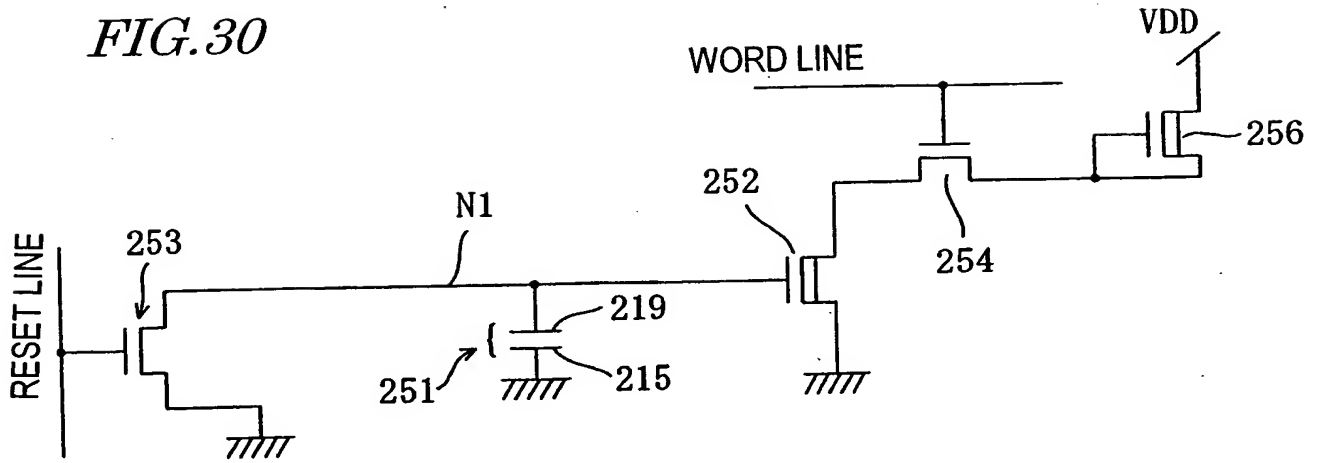


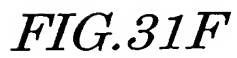
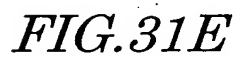
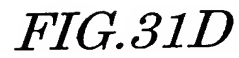
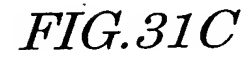
FIG. 1C is a cross-sectional view of a semiconductor device. The device is built on a substrate 201. A central stack of layers is shown, including a bottom layer 210, a middle layer 211, and a top layer 212. This stack is flanked by side regions 213 and 215. A central region 218 is located above the stack. Various layers and regions are labeled with numbers and letters: 201, 210, 211, 212, 213, 215, 216, 218, 219, 220, 222a, 223, 230a, Rse, Rc, and Rwl.

A cross-sectional view of a semiconductor device. It features a central core with a spiral pattern, surrounded by a thick layer. The spiral pattern is labeled  $R_{se}$  and  $R_{wl}$ . The thick layer is labeled  $R_c$ . The central core is labeled  $230a$  and  $230b$ .

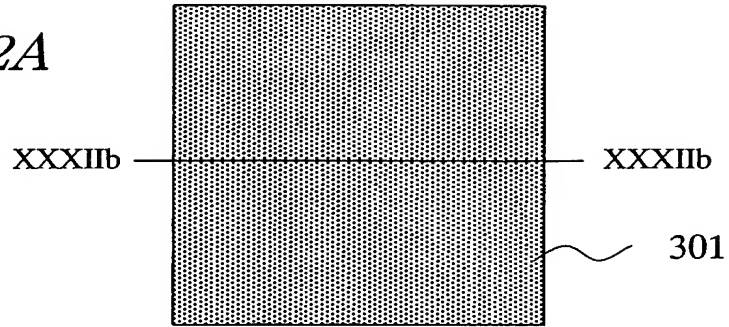
FIG. 30



*FIG. 31B*



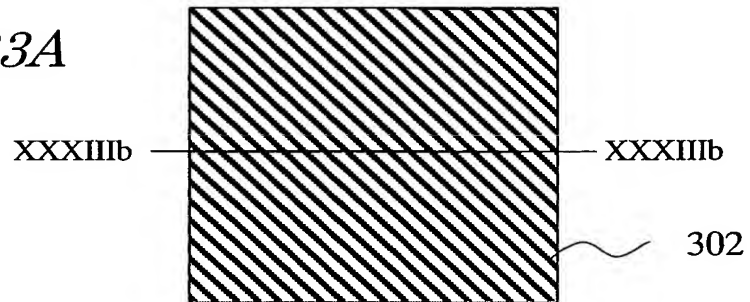
*FIG. 32A*



*FIG. 32B*



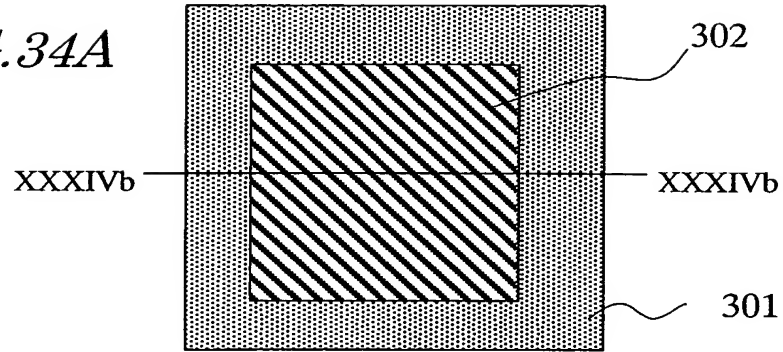
*FIG. 33A*



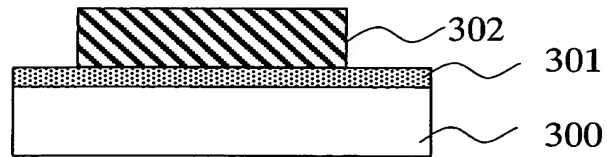
*FIG. 33B*



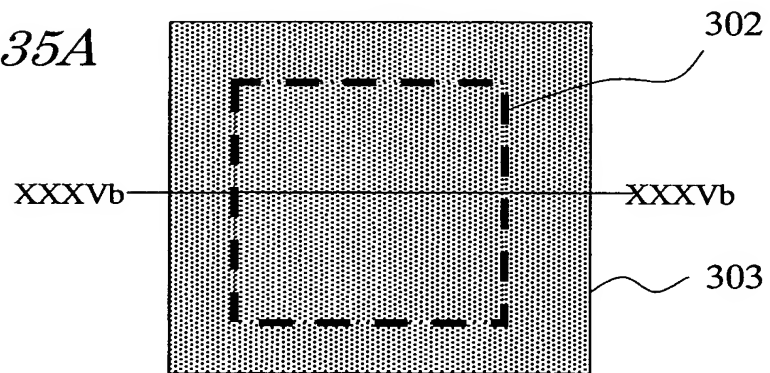
*FIG. 34A*



*FIG. 34B*



*FIG. 35A*



*FIG. 35B*

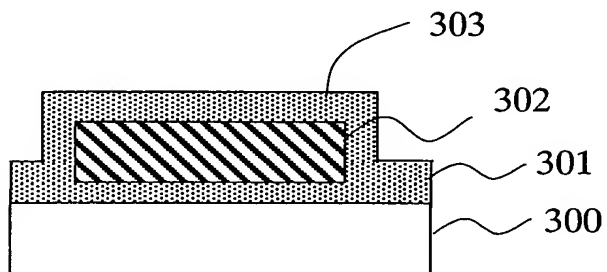


FIG. 36A

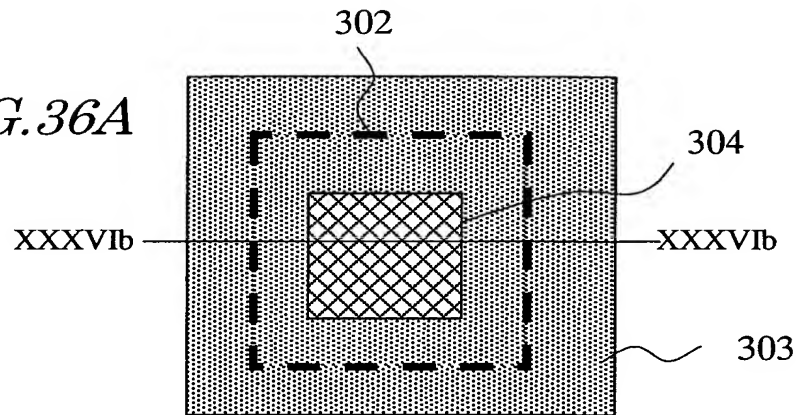


FIG. 36B

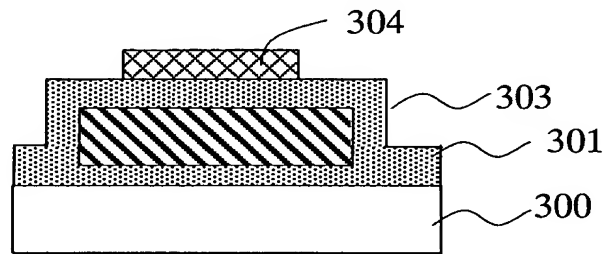


FIG. 37A

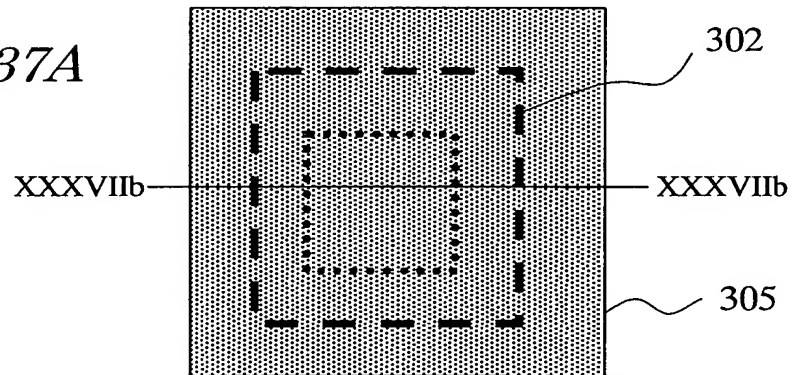


FIG. 37B

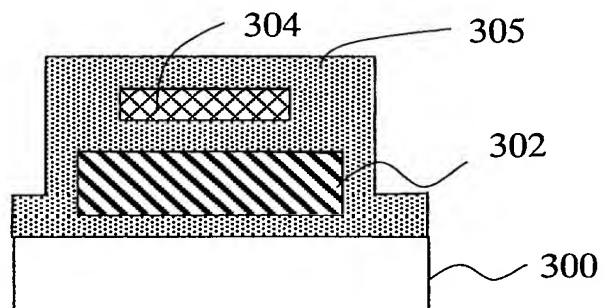


FIG. 38A

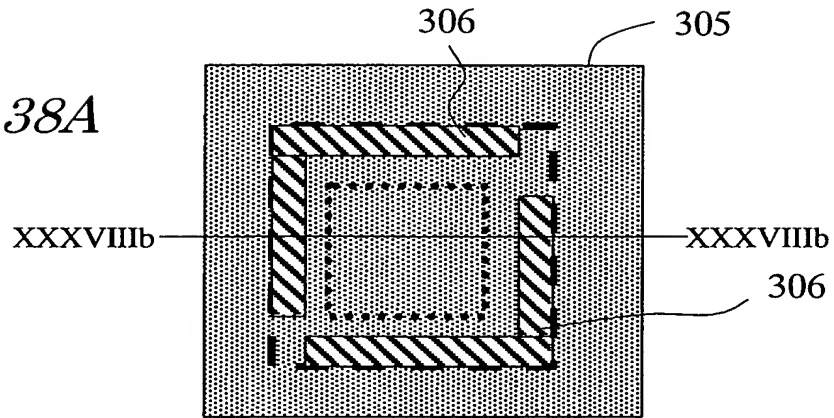


FIG. 38B

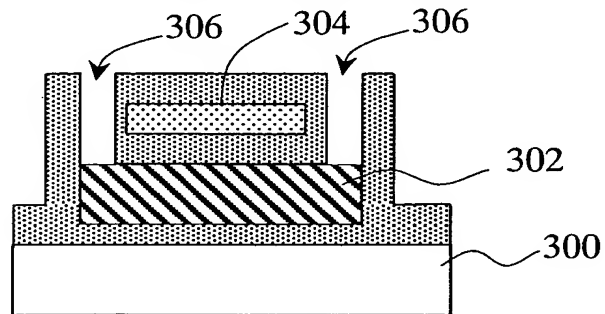


FIG. 39A

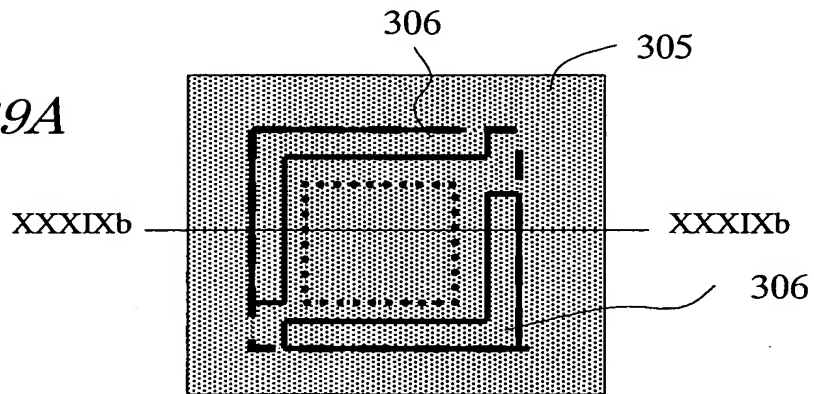
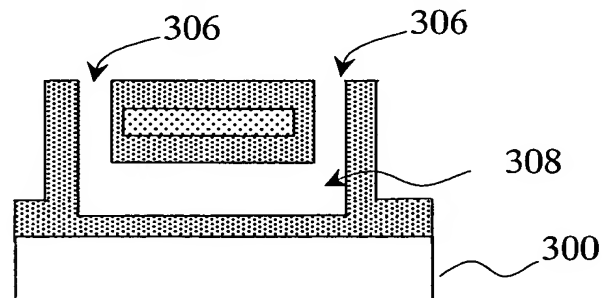
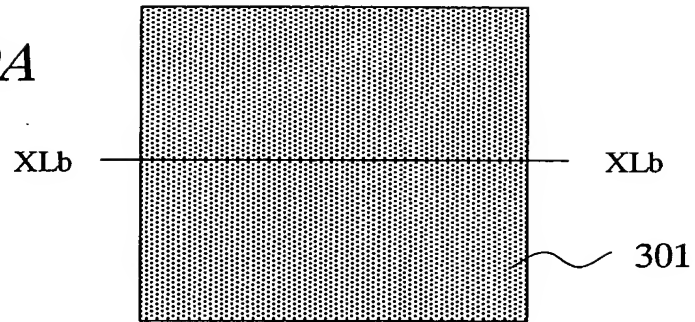


FIG. 39B





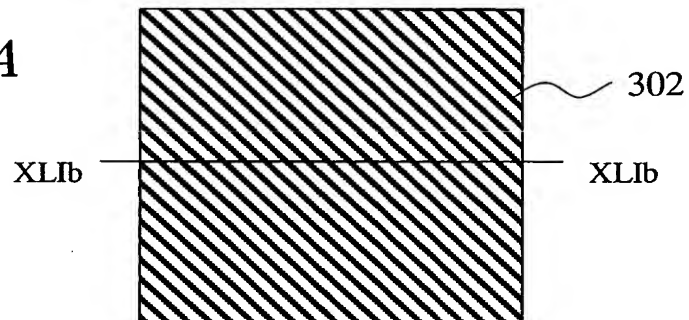
*FIG. 40A*



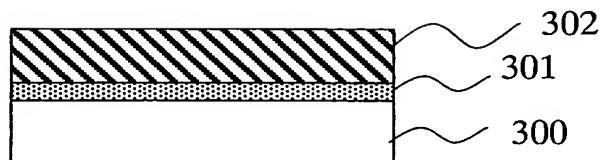
*FIG. 40B*

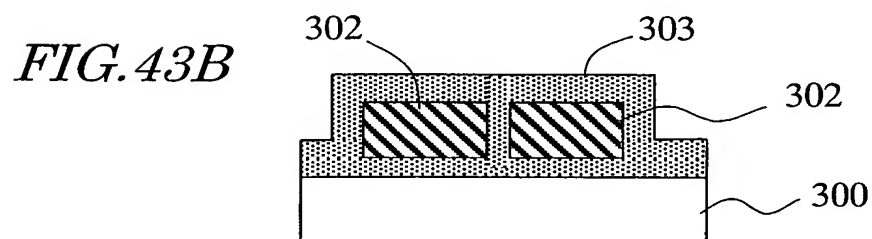
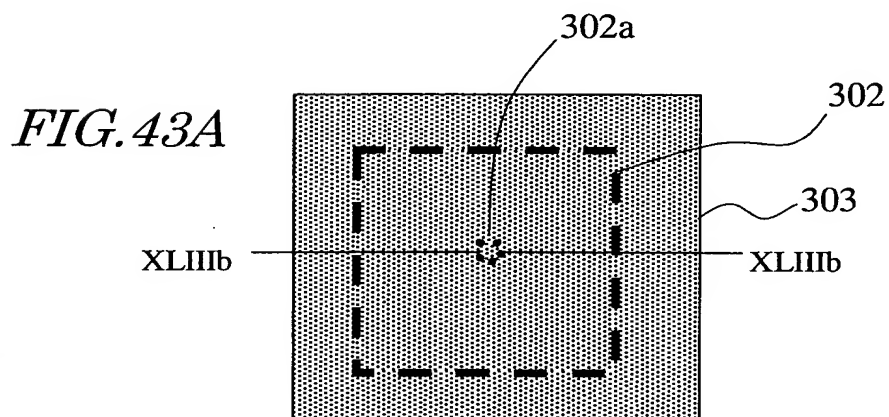
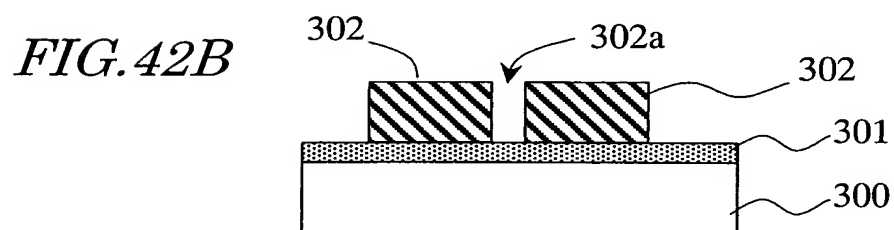
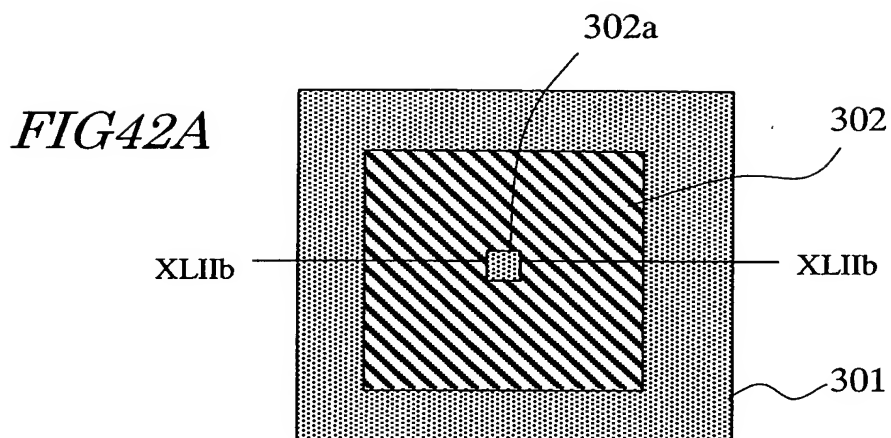


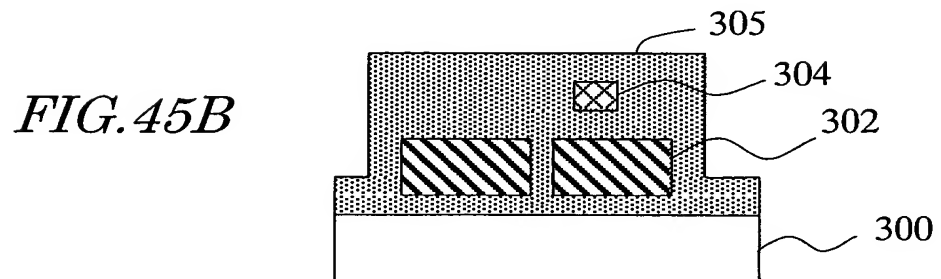
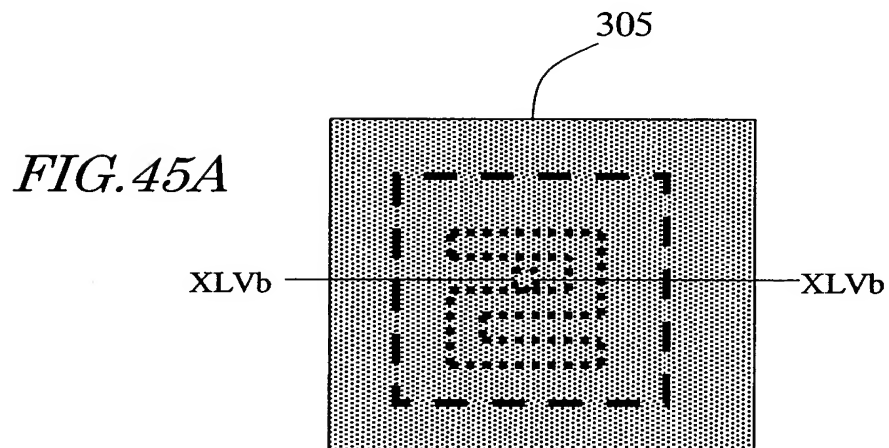
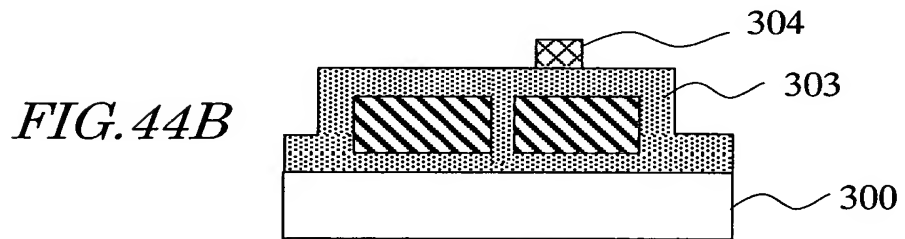
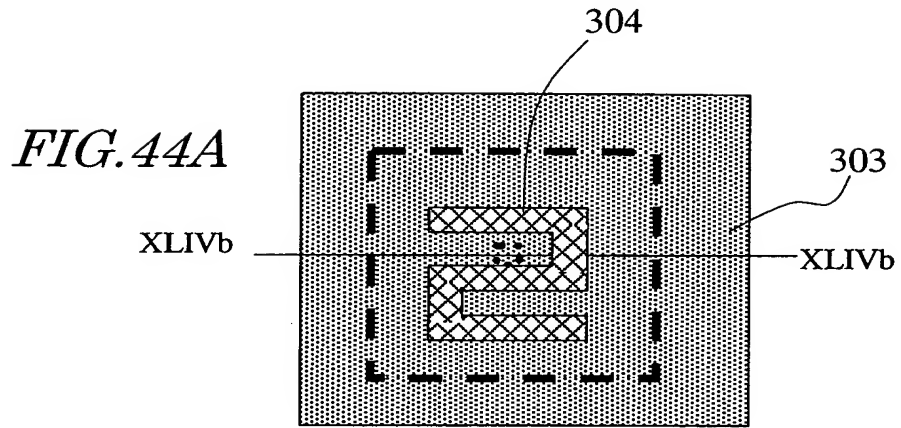
*FIG. 41A*



*FIG. 41B*







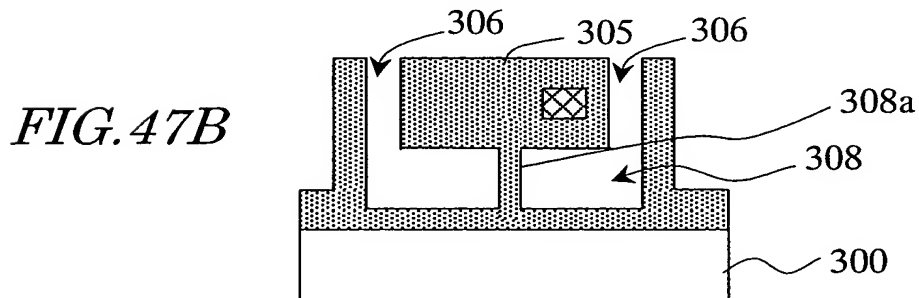
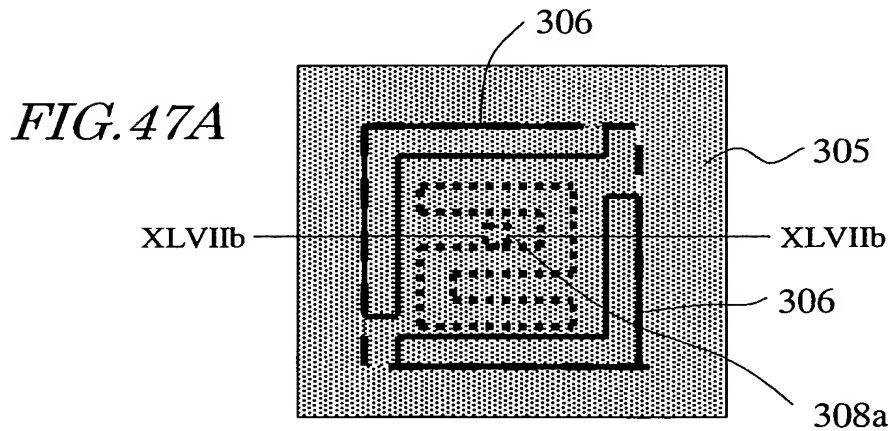
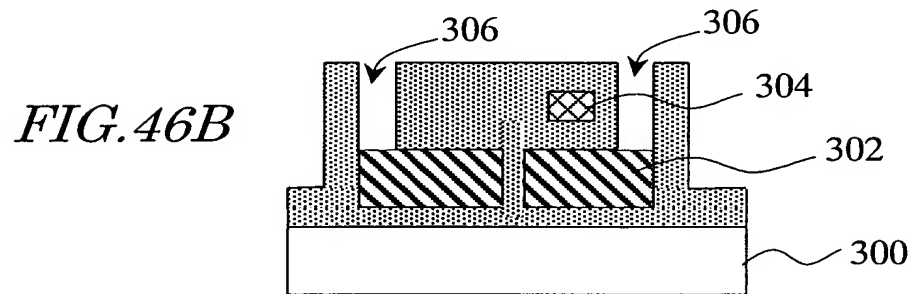
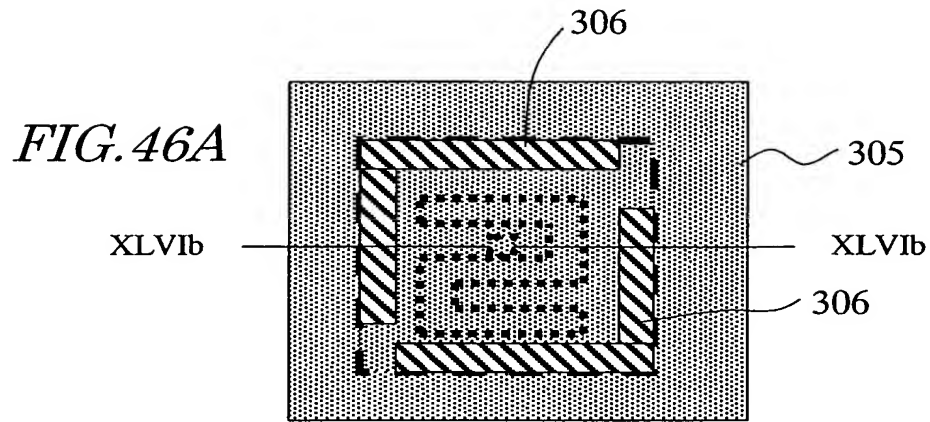


FIG. 48A

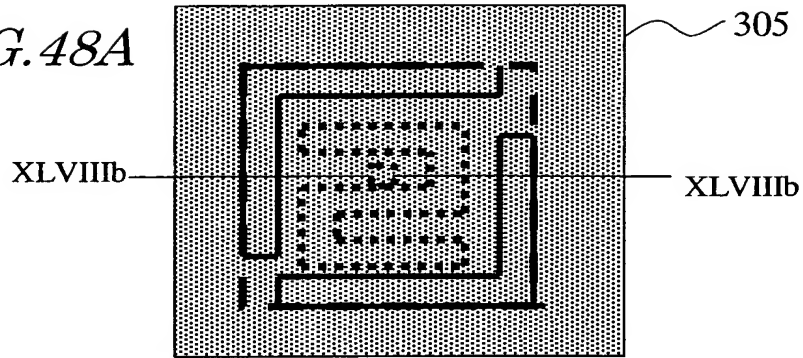


FIG. 48B

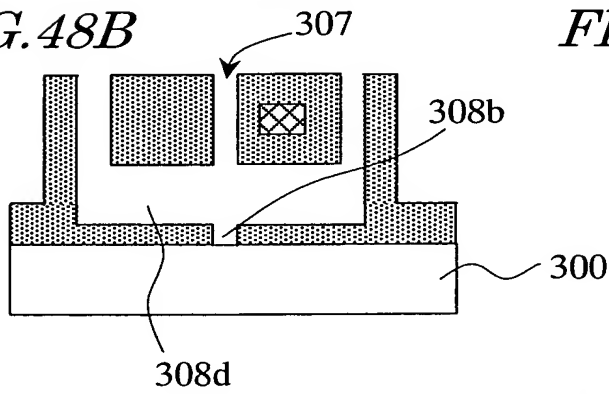


FIG. 48C

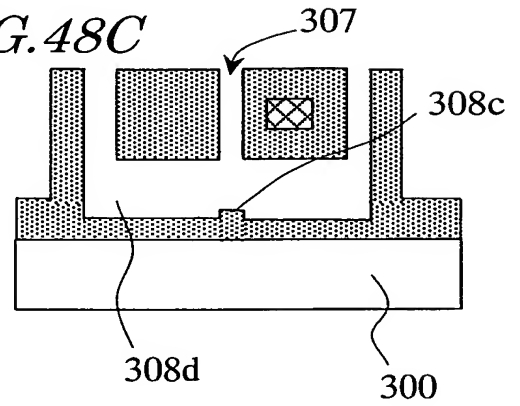


FIG. 49A

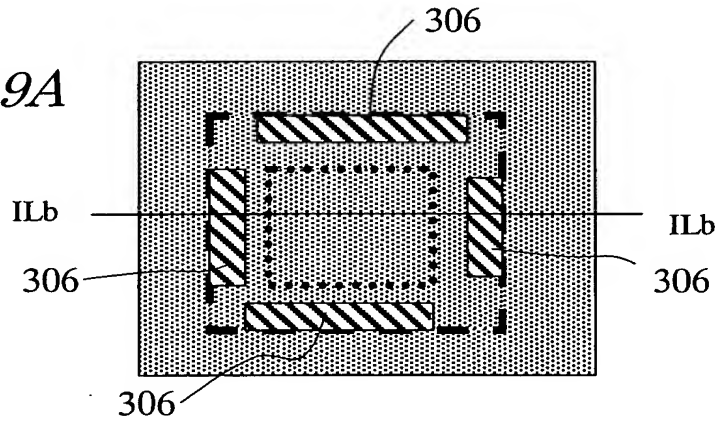
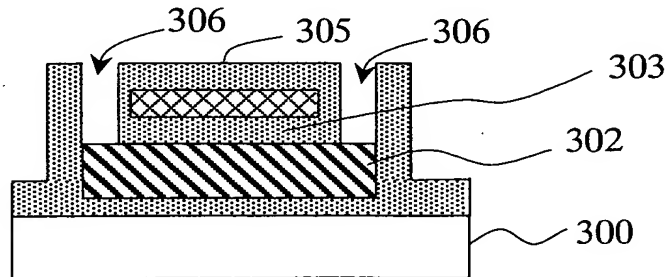
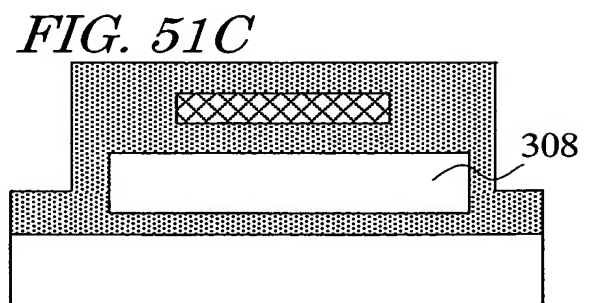
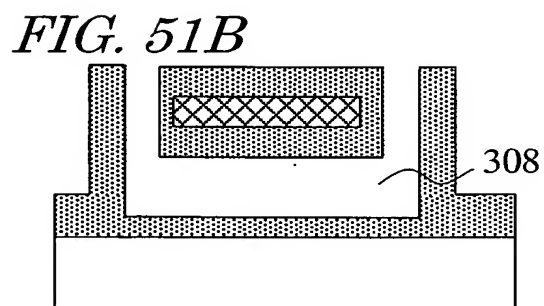
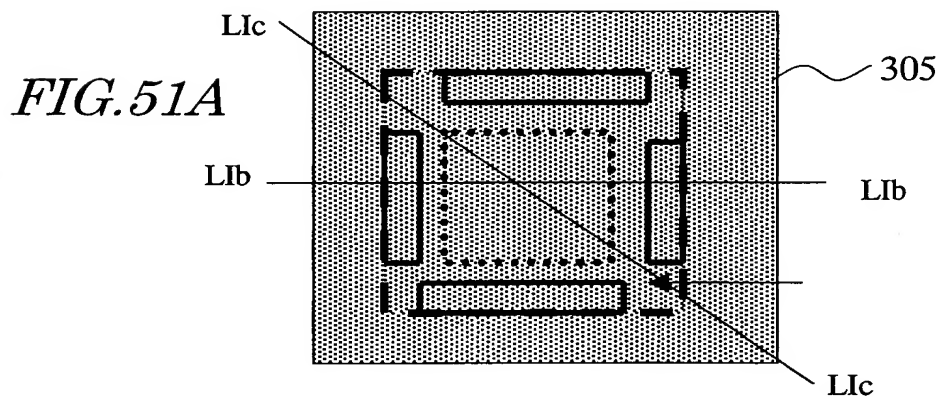
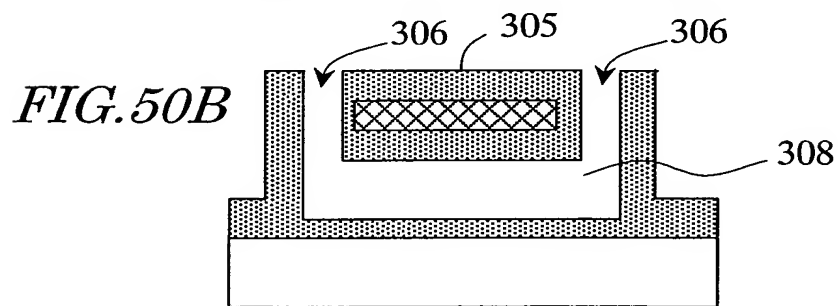
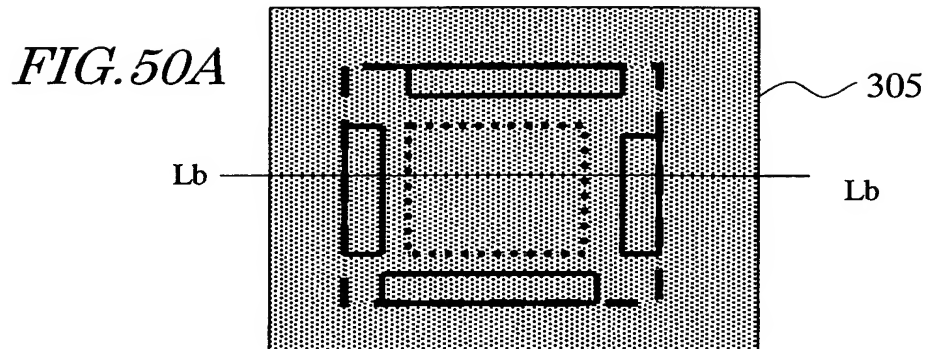
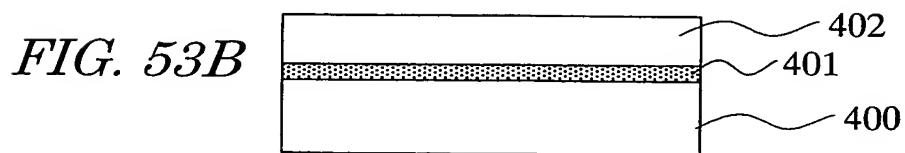
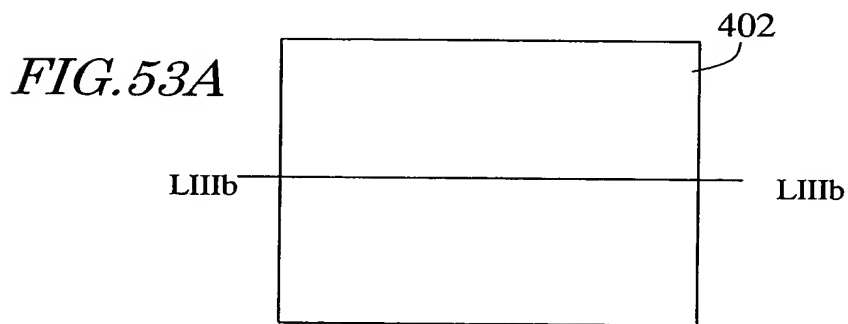
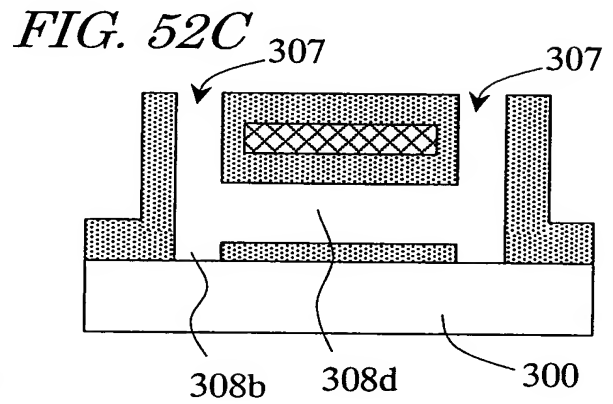
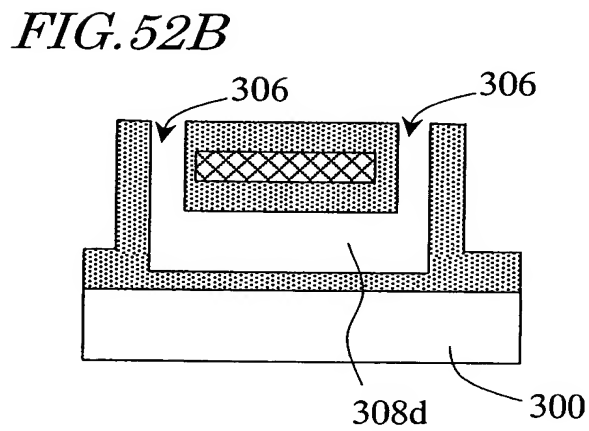
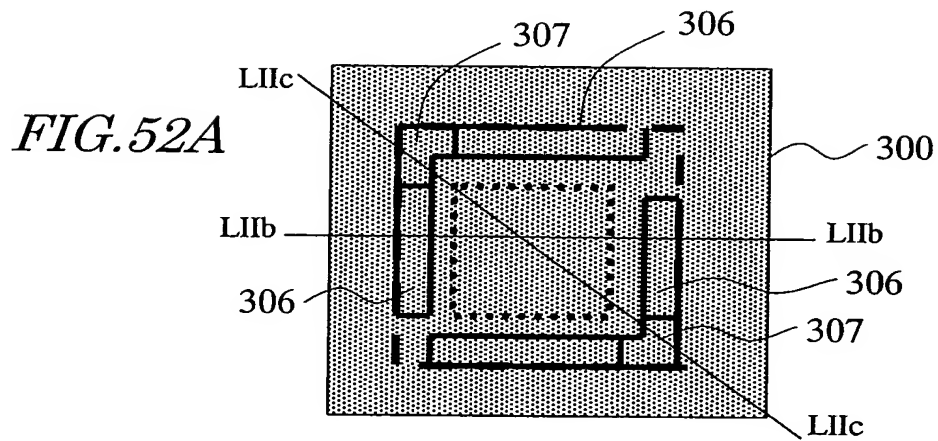
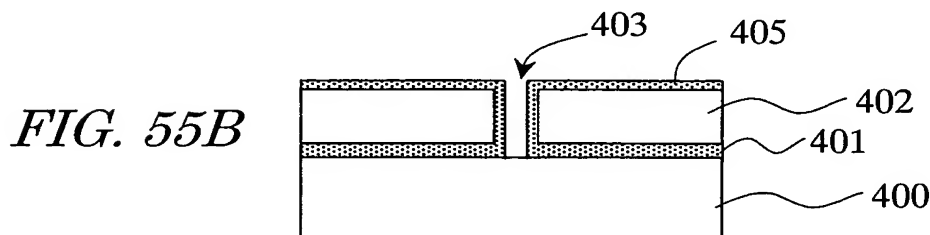
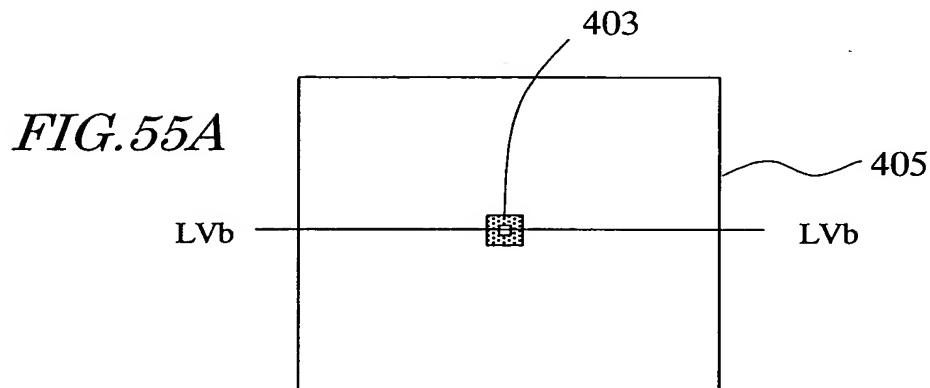
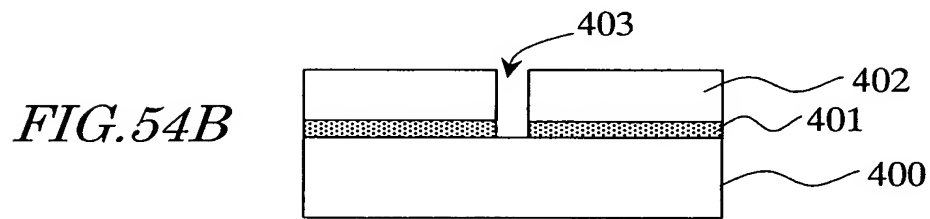
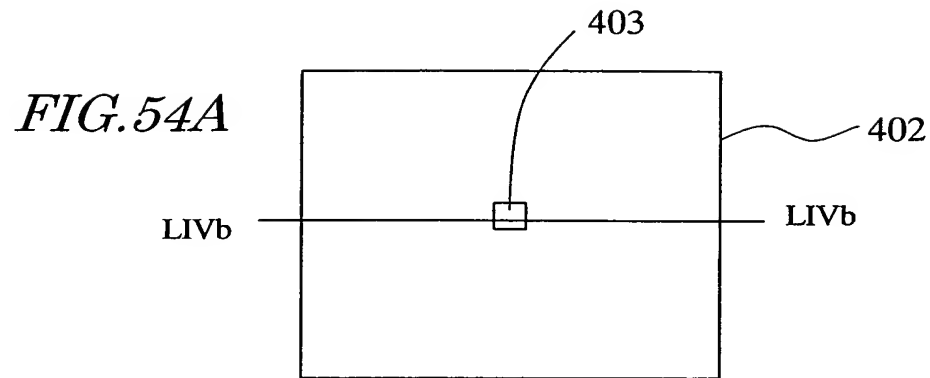


FIG. 49B

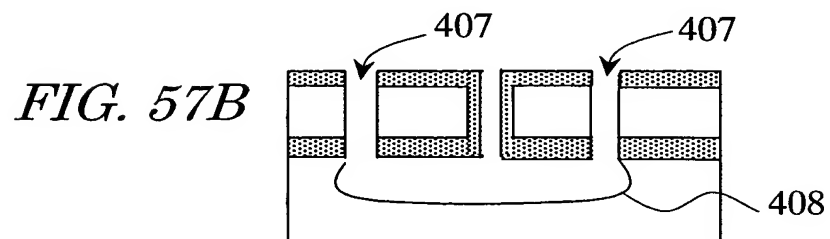
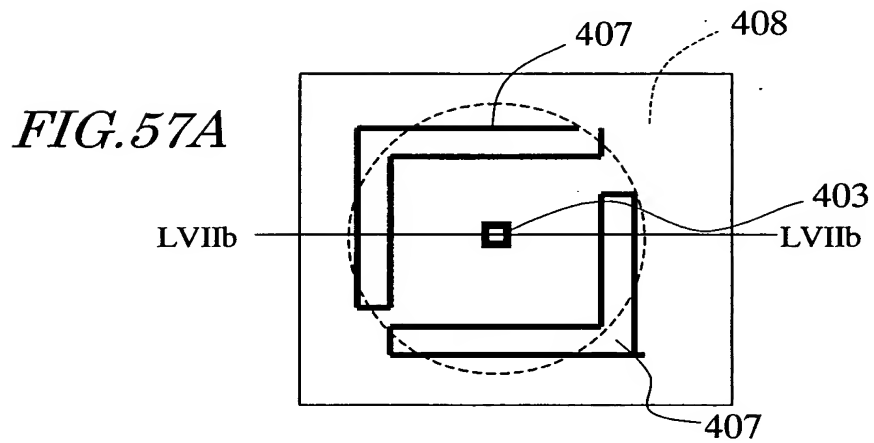
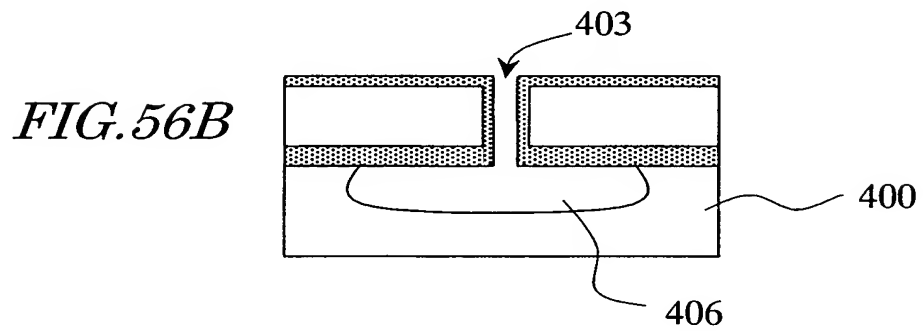
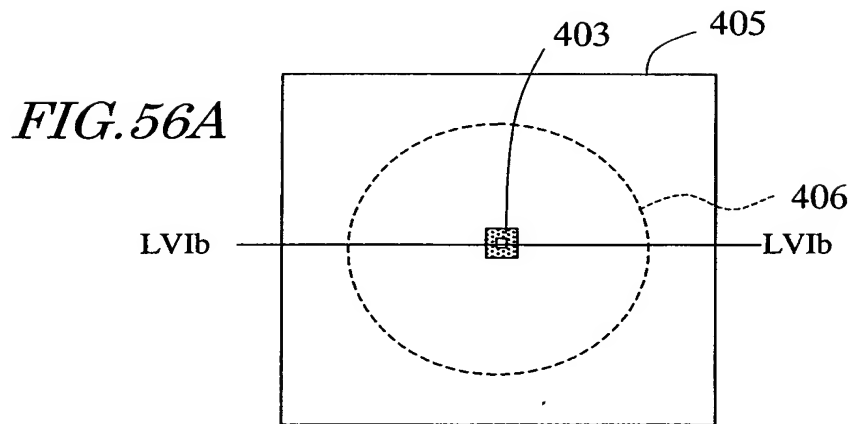




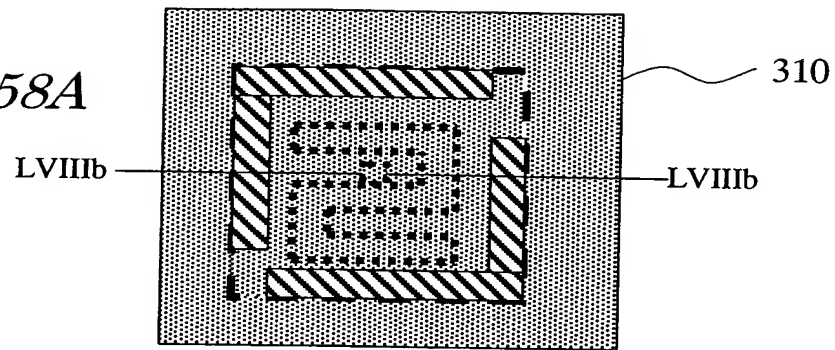




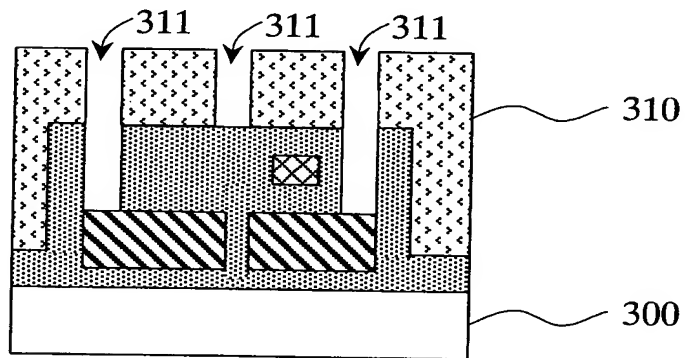




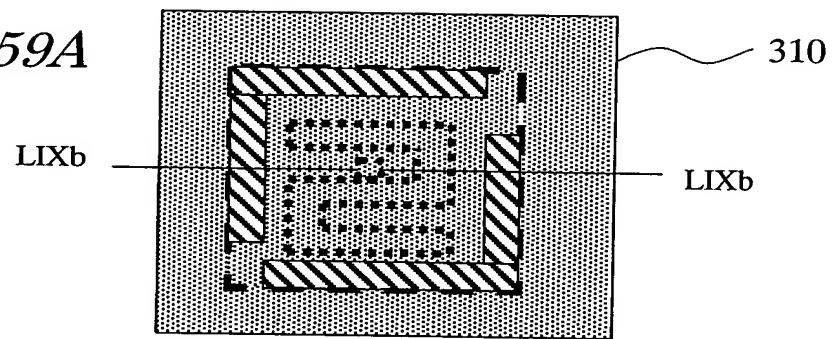
*FIG. 58A*



*FIG. 58B*



*FIG. 59A*



*FIG. 59B*

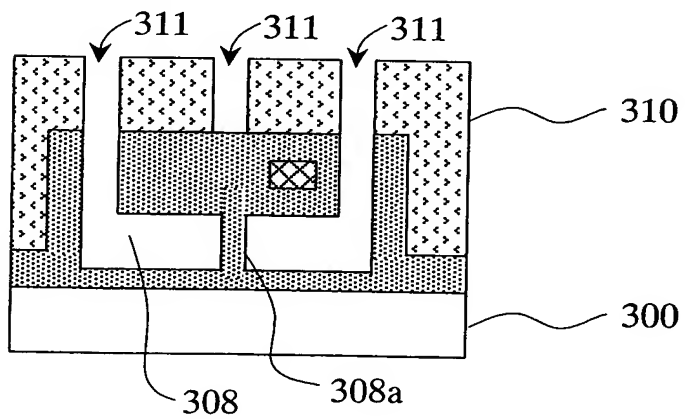


FIG. 60A

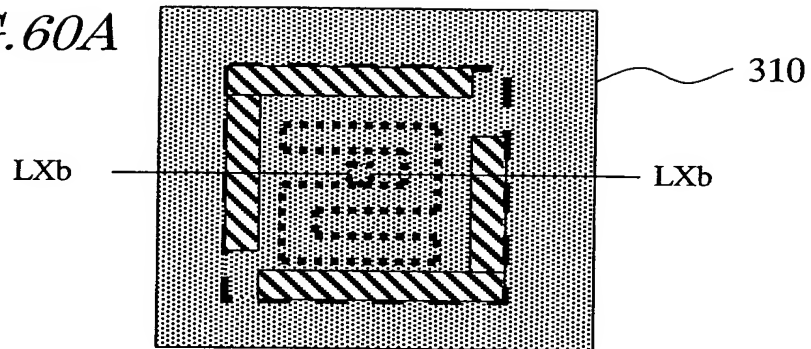


FIG. 60B

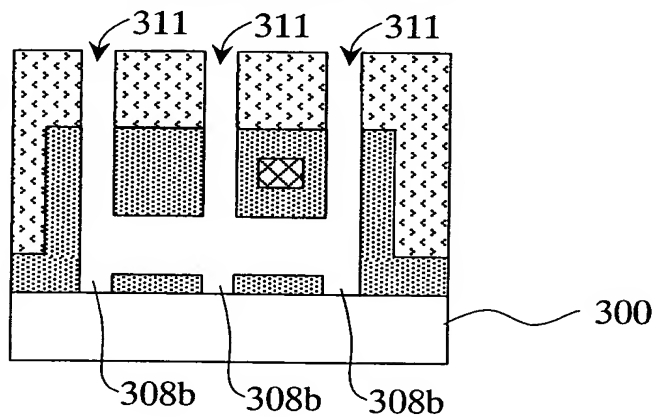


FIG. 61A

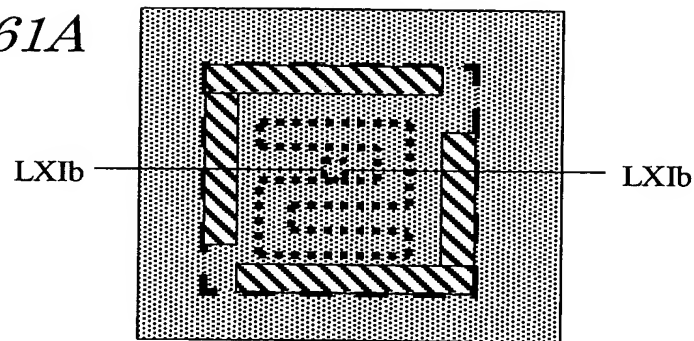


FIG. 61B

